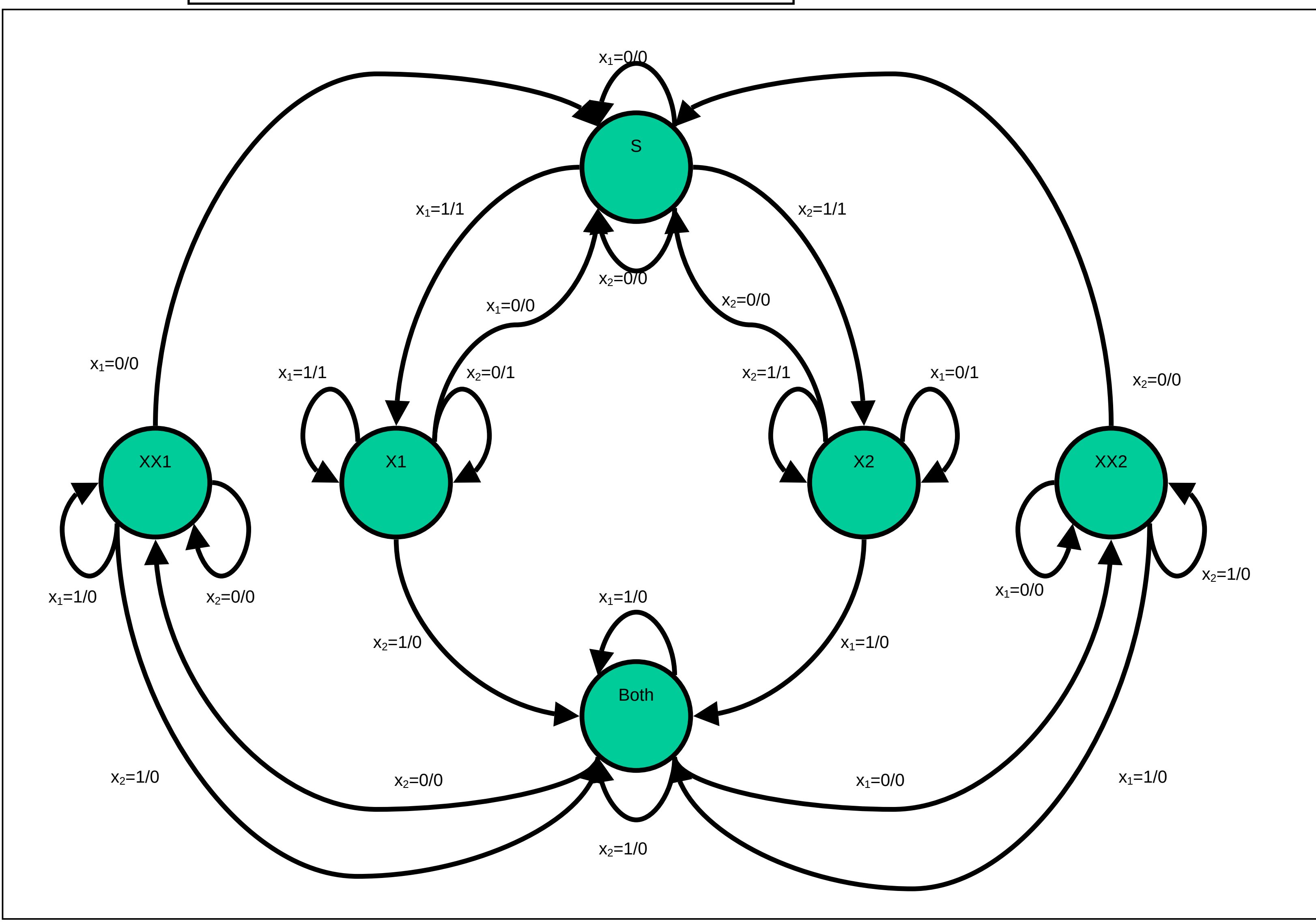
Homework 14 – due 6/28

9-14) It is necessary to design an asynchronous sequential circuit with two inputs, x_1 and x_2, and one output, z. Initially, both inputs and output are equal to 0. When x_1 or x_2 becomes 1, z becomes 1. When the second input also becomes 1, the output changes to 0. The output stays at 0 until the circuit goes back to the initial state.

a) Obtain a primitive flow table for the circuit and show that it can be reduced to the flow table shown in Fig P9-14.

b) Complete the design of the circuit.

	00	01	11	10
a	a,0	a,1	b,-	a,1
b	a,-	b,	b,	b,



This is the primitive flow table:

State	Inputs: x_1x_2			
	00	01	11	10
S	S/0	X2/1	-	X1/1
X1	S/0	-	Both/0	X1/1
X2	S/0	X2/1	Both/0	-
Both	-	XX2/0	Both/0	XX1/0
XX1	S/0	-	Both/0	XX1/0
XX2	S/0	XX2/0	Both/0	-

S, X1, and X2 can be merged, as can Both, XX1, and XX2. The resulting flow table is:

State	Inputs: x_1x_2			
	00	01	11	10
S	S/0	S/1	Both/0	S/1
Both	S/0	Both/0	Both/0	Both/0

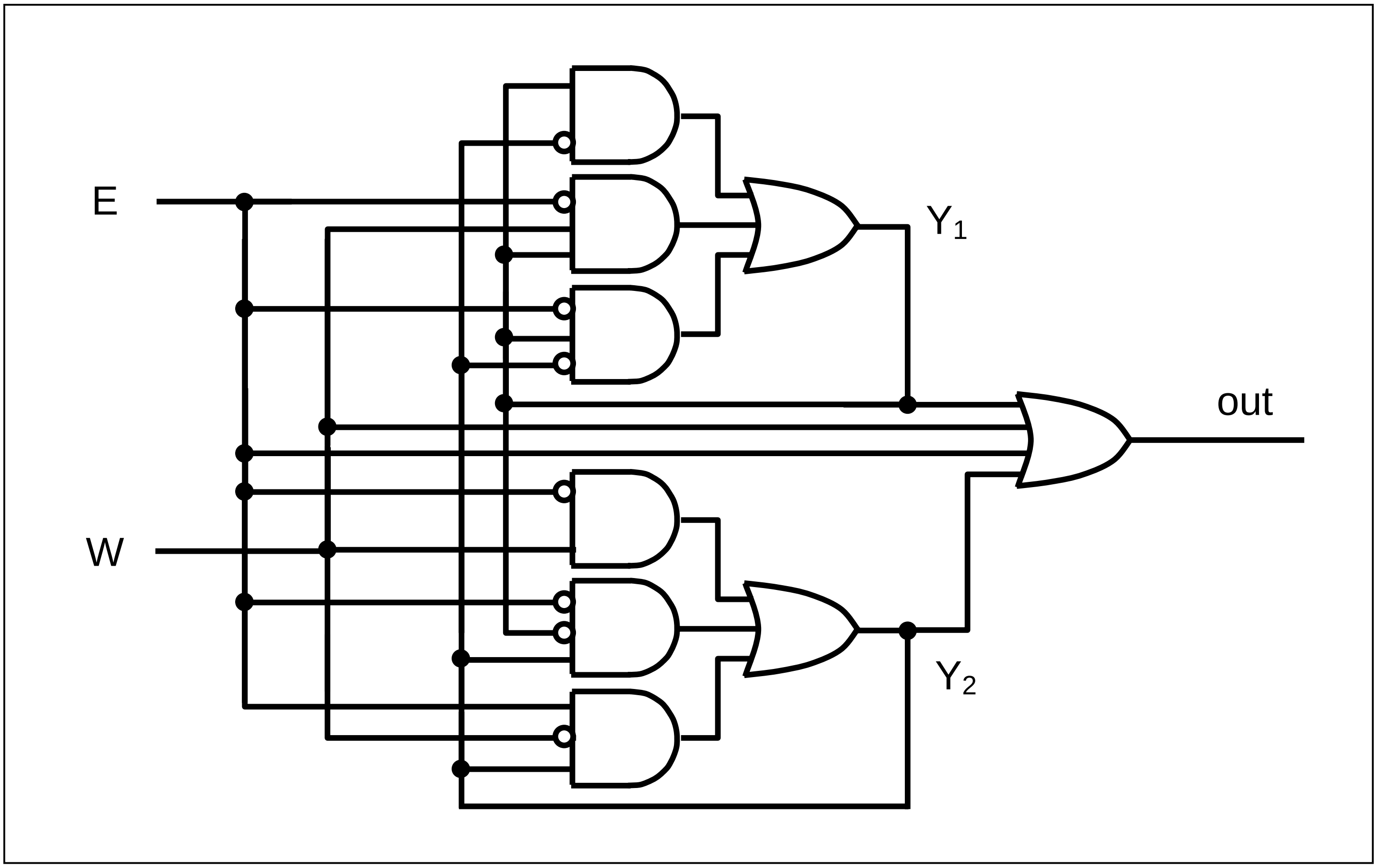
Relabeling the state names:

State	Inputs: x_1x_2			
	00	01	11	10
a	a/0	a/1	b/0	a/1
b	a/0	b/0	b/0	b/0

This is equivalent to the figure.

Verify the solution to problem 9-13 by analyzing the circuit and comparing resulting transition table to problem definition.

Here is the circuit diagram:



First, verify the transition equations from the diagram:

$Y_1 = y_1y_2' + y_1E'W + y_1y_2'E'$
$Y_2 = E'W + y_1'y_2E' + y_2EW'$
$\text{Output} = y_1 + y_2 + E + W$

These match the design equations.

Next, find the excitation functions:

y_1y_2\EW	00	01	11	10
00				
01				
11		1		
10	1	1	1	1

Y_1

y_1y_2\EW	00	01	11	10
00		1		
01	1	1		1
11		1		1
10		1		

Y_2

Y_2 matches, but Y_1 does not. The proper equation for Y_1 should be:
$Y_1 = EW' + E'Wy_1 + E'y_1y_2$

Now, we would have a transition table (shaded cells are stable states):

y_1y_2\EW	00	01	11	10
00	00,0	01,1	00,1	10,1
01	01,1	01,1	00,1	11,1
11	00,1	11,1	00,1	11,1
10	10,1	11,1	00,1	10,1

Y_1Y_2

Note: y_1y_2 = 10 with input 01 was marked as a stable state. It isn't.

Now, verify that the system performs as intended:
Case 1) a train approaches from the East.

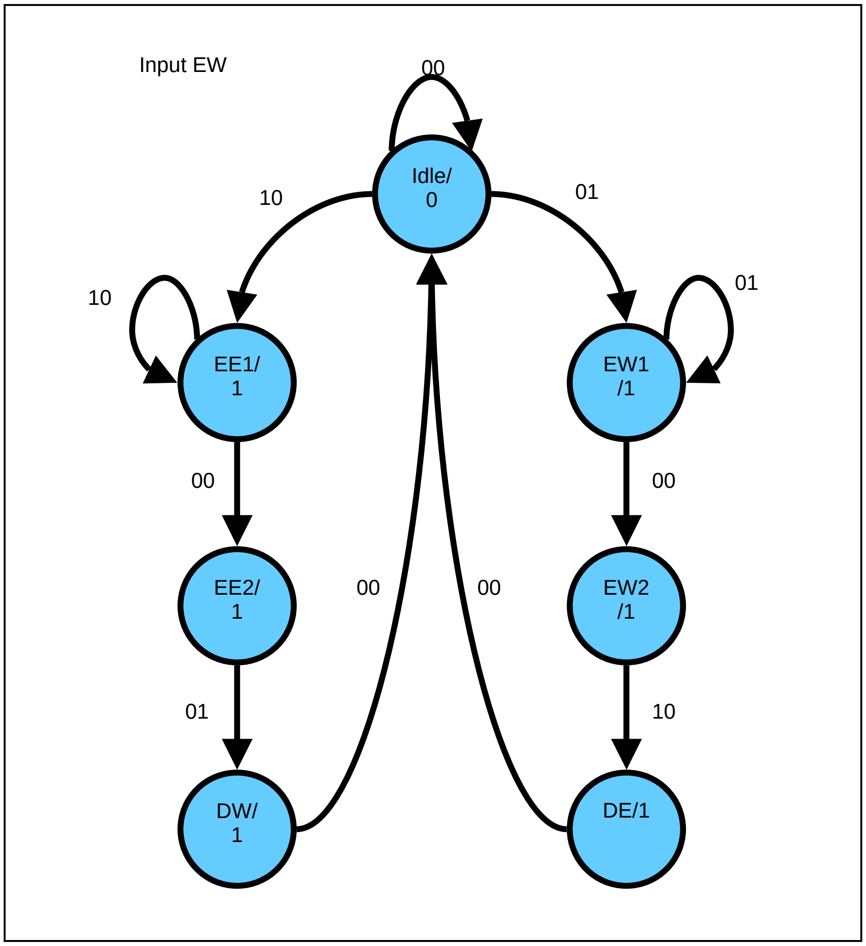
1. The system is in state 00 with 00 input
2. The E sensor is activated (input 10).
3. Output 1, system goes to state 10, stable state. (gate closes)
4. E sensor is released (input 00). System stays in state 10.
5. W sensor is activated as train leaves section (input 01). System goes to state 11 with 1 output – stable state.
6. W sensor is released (input 00). System goes to state 00 with 1 output.
7. System is in stable state 00 with 00 input. Output goes to 0 (gate opens)

Case 2) a train approaches from the West

1. The system is in state 00 with 00 input
2. The W sensor is activated (input 01).
3. Output 1, system goes to state 01, stable state. (gate closes)
4. W sensor is released (input 00). System stays in state 01.
5. E sensor is activated as train leaves section (input 10). System goes to state 11 with 1 output – stable state.
6. E sensor is released (input 00). System goes to state 00 with 1 output.
7. System is in stable state 00 with 00 input. Output goes to 0 (gate opens)

Redo problem 9-13 with a synchronous design. Assume that a clock exists with a 1 second period.

First, we start with a state diagram, as shown below.



From this, we can generate a state table:

	Input (EW)				
State	00	01	11	10	Output
Idle	Idle	EW1	-	EE1	0
EE1	EE2	-	-	EE1	1
EW1	EW2	EW1	-	-	1
EE2	EE2	DW	-	-	1
EW2	EW2	-	-	DE	1
DW	Idle	DW	-	-	1
DE	Idle	-	-	DE	1

States EE1 and EW1 can be merged, as can EW1 and EW2. Likewise, states DW and DE can also be merged. Here is the reduced state table:

	Input EW				
State	00	01	11	10	Output
Idle	Idle	EW	-	EE	0
EE	EE	D	-	EE	1
EW	EW	EW	-	D	1
D	Idle	D	-	D	1

If we perform a simple state assignment:

	Input EW				
State	00	01	11	10	Output
00	00	01	X	10	0
01	01	01	X	11	1
11	00	11	X	11	1
10	10	11	X	10	1

Next, we can compute the inputs needed to realize this system with D FFs:

AB\EW	00	01	11	10
00	0	0	X	1
01	0	0	X	1
11	0	1	X	1
10	1	1	X	1

$D_A = E + AB' + AW$

AB\EW	00	01	11	10
00	0	1	X	0
01	1	1	X	1
11	0	1	X	1
10	0	1	X	0

$D_B = W + A'B + BE$

Here is the resulting circuit: