

9-6) Investigate the transition table of Fig P9-6 and determine all race conditions and whether they are critical or noncritical. Also determine whether there are any cycles.

	x_1x_2			
y_1y_2	00	01	11	10
00	10	00	11	10
01	01	00	10	10
11	01	00	11	11
10	11	00	10	10

From state 00, with input 01, the system is in a stable state. There are two possible changes in input that would be allowed: 00 or 11. With input 00, the system will transit states 10, 11, and 01, ultimately ending in state 01, which is a stable state. There is no race here. With input 11, the next state is 11, which requires the change of two state variables. Thus, a race exists. The next state could be 01, 10, or 11. If the next state is 01, this causes a transition to 10, which is a stable state. If the next state is 10, this is the same stable state. However, if the next state is 11, this is a different stable state, thus, this is a critical race.

From state 01, with input 00, the system is in a stable state. There are two possible input conditions that would be allowed: 01 or 10. With input 01, the system goes directly to state 00, which is a stable state. With input 10, the system is sent to state 10, which requires a change in two state variables, thus a race condition exists. Potential next states are 00, 10, or 11. If the next state is 00, this forces a transition to 10, which is a stable state. If the next state is 10, this forces the system to the same stable state. However, if the next state is 11, this is a different stable state. Thus, this is also a critical race.

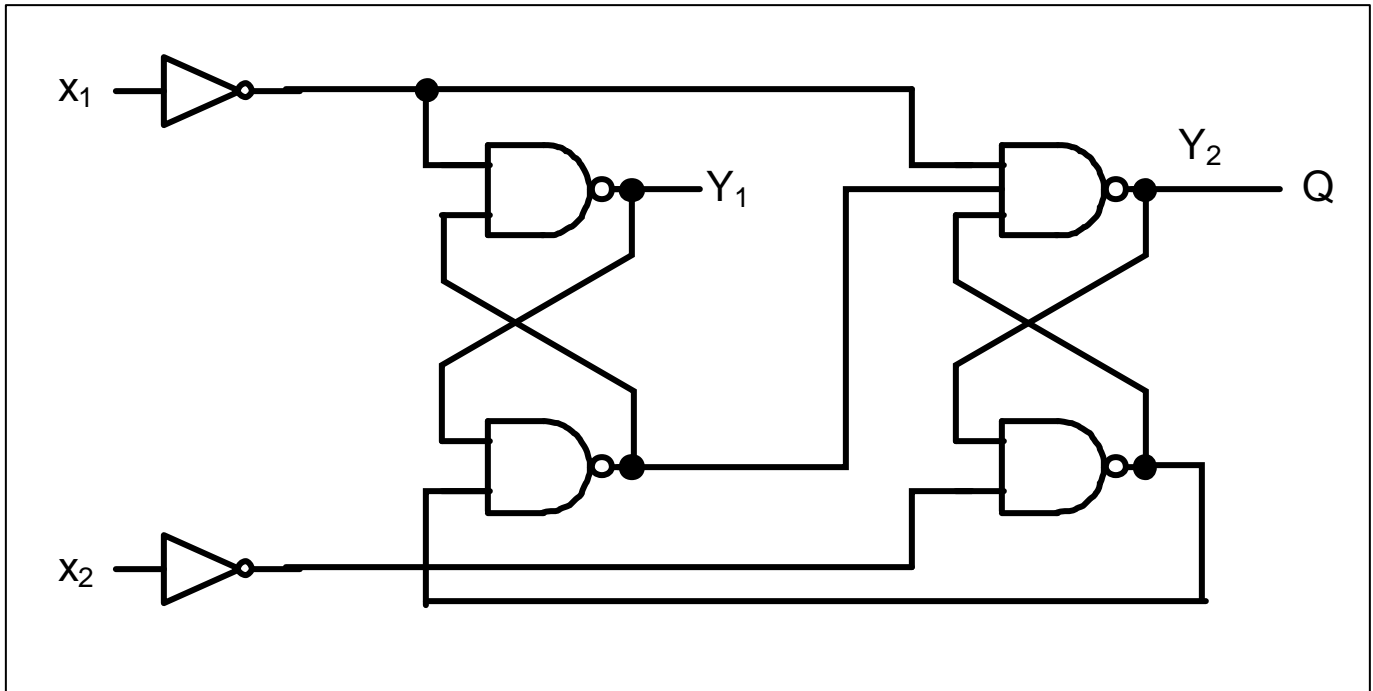
From state 10, there are two stable input conditions – with input 10 or 11. If the input is 10, there are two possible input changes that are possible – input 00 or input 11. If the input changes to 00, the next state is 11, a 1 bit change. 11 goes to 01, which is a stable state. Thus, this condition has no races. If the input changes to 11, this is also a stable state for state 10, so there is no change and no race.

From state 11, there are two stable input conditions – with input 10 or 11. If the input were 10, there are two possible next values for the input: 00 and 11. If the input changes to 00, the next state is 11, a one bit change in state variables. This leads to state 01, another 1 bit change, leading to a final stable state of 01. If the input changes to 11, there is no change of state, so there are no races. If the input were 11, there are two possible changes of input: to 01 or 10. If the input changes to 01, the next state is 00, causing a 2-bit change in state variables and a race condition. However, for input 01, all states lead directly to 00, so there is no critical race condition. If the input changes to 10, the next state is 11, so there is no race condition.

There are no cycles for this system

9-9) For the asynchronous circuit show in Fig P9-9,

- Derive the Boolean functions for the outputs of the two SR latches Y_1 and Y_2 . Note that the S input of the second latch is $x_1'y_1'$.
- Derive the transition table and output map of the circuit.



$$\begin{aligned} S_1 &= x_1' \\ R_1 &= y_2' \\ S_2 &= x_1'y_1' \\ R_2 &= x_2' \end{aligned}$$

The condition for correct behavior of the latches requires that $S'R' = 0$.
 This means that $x_1y_2 = 0$ (latch 1) and $(x_1'y_1')'x_2 = x_1x_2 + y_1x_2 = 0$ (latch 2)

Using the latch operation equation: $Y = S' + Ry$,
 $Y_1 = x_1 + y_1y_2'$ as long as $x_1y_2 = 0$ and
 $Y_2 = x_1 + y_1 + x_2'y_2$ as long as $x_1x_2 + y_1x_2 = 0$

Eliminating the cases that are prevented by the SR conditions, the transition table will not be allowed to use the dashed cells.

$y_1y_2 \backslash x_1x_2$	00	01	11	10
00			-	
01			-	-
11		-	-	-
10		-	-	

Next, fill in the remaining conditions with the definitions of Y_1Y_2 . Stable states are shaded in red:

$y_1y_2 \backslash x_1x_2$	00	01	11	10
00	00	00	-	11
01	01	00	-	-
11	01	-	-	-
10	11	-	-	11