

Homework 9 – due 6/16

5-16) Design a sequential circuit with two D FFs, A and B, and one input x. When x = 0, the state of the circuit remains the same. When x = 1, the circuit goes through the state transitions from 00 to 01 to 11 to 10 back to 00 and repeats.

State		Input	Next state	
A	B	x	A	B
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	1	0
1	0	1	1	1
1	1	0	1	1
1	1	1	0	0

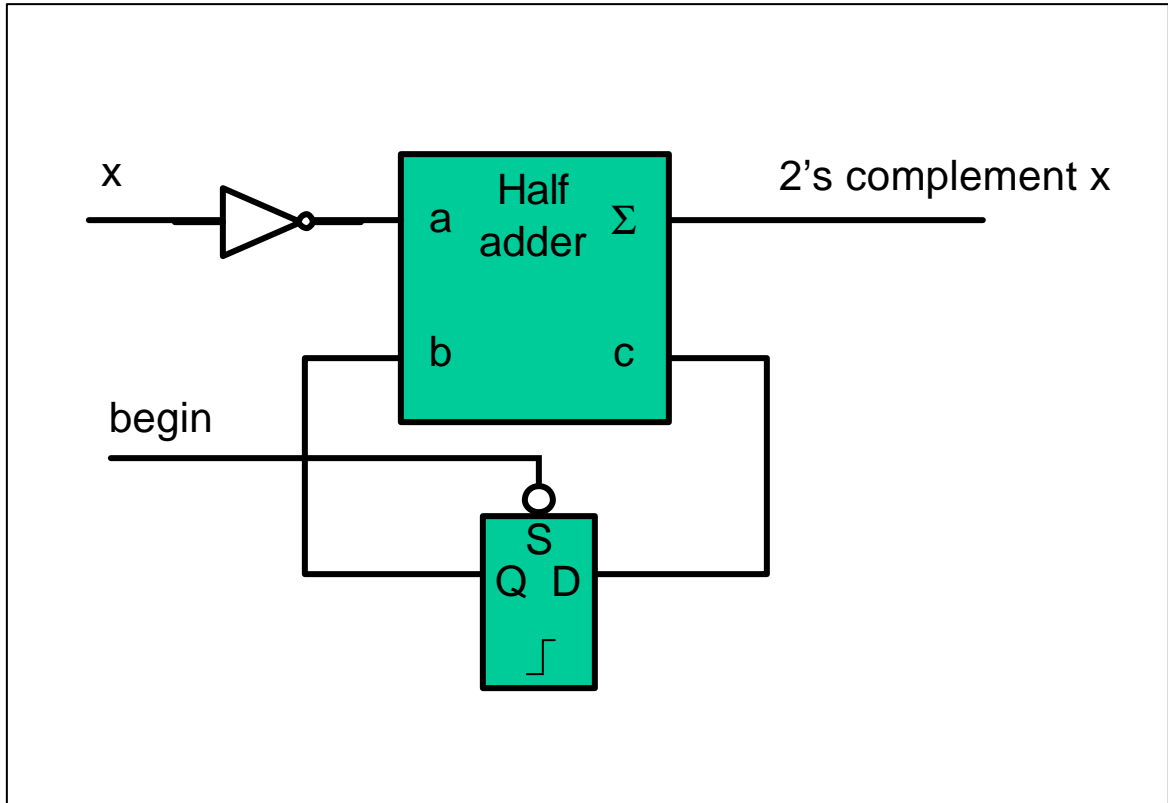
x\AB	00	01	11	10
0	0	0	1	1
1	0	1	0	1

$$D_A = x'A + AB' + xA'B$$

x\AB	00	01	11	10
0	0	1	1	0
1	1	0	0	1

$$D_B = x'B + xB'$$

5-17) Design a one input, one output serial 2's complementer. The circuit accepts a string of bits from the input and generates the 2's complement at the output. The circuit can be reset asynchronously to start and end the operation.



This circuit implements the serial 2's-complement operation. Before the first bit of x is shifted in, the FF is set to 1, representing the 1 that gets added to the number. x is shifted in, LSB first, with each bit complemented as it is added. Since this circuit only has 1 input, it is not necessary to use a full adder – a half adder will do, since the only inputs are x and the carry result from lower order bits.

5-18) Design a sequential circuit with two JK FFs A and B and two inputs E and x. If E=0, the circuit remains in the same state, regardless of the value of x. When E = 1 and x = 1, the circuit goes through the state transitions from 00 to 01 to 10 to 11 back to 00, and repeats. When E = 1 and x = 0, the circuit goes through the state transitions from 00 to 11 to 10 to 01 and back to 00, and repeats.

State		Input		Next		Controls			
A	B	E	X	A	B	J _A	K _A	J _B	K _B
0	0	0	0	0	0	0	X	0	X
0	0	0	1	0	0	0	X	0	X
0	0	1	0	1	1	1	X	1	X
0	0	1	1	0	1	0	X	1	X
0	1	0	0	0	1	0	X	X	0
0	1	0	1	0	1	0	X	X	0
0	1	1	0	0	0	0	X	X	1
0	1	1	1	1	0	1	X	X	1
1	0	0	0	1	0	X	0	0	X
1	0	0	1	1	0	X	0	0	X
1	0	1	0	0	1	X	1	1	X
1	0	1	1	1	1	X	0	1	X
1	1	0	0	1	1	X	0	X	0
1	1	0	1	1	1	X	0	X	0
1	1	1	0	1	0	X	0	X	1
1	1	1	1	0	0	X	1	X	1

Q(t)	J	K	Q(t+1)
0	0	X	0
0	1	X	1
1	X	1	0
1	X	0	1

AB\Ex	00	01	11	10
00	0	0	0	1
01	0	0	1	0
11	X	X	X	X
10	X	X	X	X

$$J_A = BEx + B'Ex'$$

AB\Ex	00	01	11	10
00	X	X	X	X
01	X	X	X	X
11	0	0	1	0
10	0	0	0	1

$$K_A = BEx + B'Ex'$$

AB\Ex	00	01	11	10
00	0	0	1	1
01	X	X	X	X
11	X	X	X	X
10	0	0	1	1

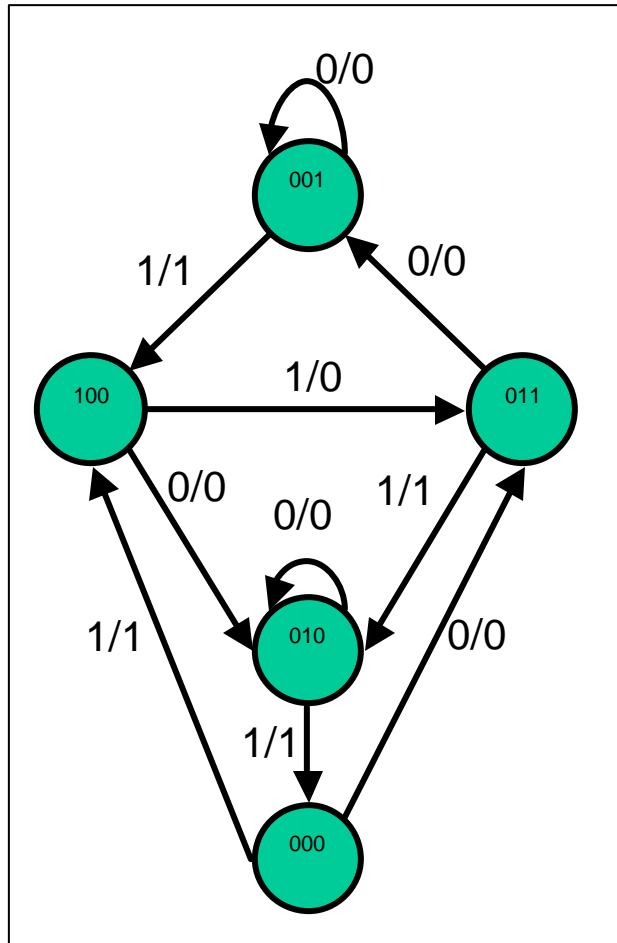
J_B = E

AB\Ex	00	01	11	10
00	X	X	X	X
01	0	0	1	1
11	0	0	1	1
10	X	X	X	X

K_B = E

5-19) A sequential circuit has three FFs A, B, C; one input x, and one output y. The state transition diagram is shown below. The circuit is to be designed by treating the unused states as don't-care conditions. Analyze the circuit obtained to determine the effect of the unused states.

- a) use D FFs in the design
- b) use JK FFs in the design



State			Input	Next state			Output
A	B	C	x	A	B	C	y
0	0	1	0	0	0	1	0
0	0	1	1	1	0	0	1
1	0	0	0	0	1	0	0
1	0	0	1	0	1	1	0
0	1	0	0	0	1	0	0
0	1	0	1	0	0	0	1
0	1	1	0	0	0	1	0
0	1	1	1	0	1	0	1
0	0	0	0	0	1	1	0
0	0	0	1	1	0	0	1

a) With D FF:

xA\BC	00	01	11	10
00	0	0	0	0
01	0	X0	X0	X0
11	0	X0	X0	X0
10	1	1	0	0

$$D_A = xA'B'$$

xA\BC	00	01	11	10
00	1	0	0	1
01	1	X1	X1	X1
11	1	X1	X1	X1
10	0	0	1	0

$$D_B = A + x'C' + xBC$$

xA\BC	00	01	11	10
00	1	1	1	0
01	0	X1	X1	X0
11	1	X1	X1	X1
10	0	0	0	0

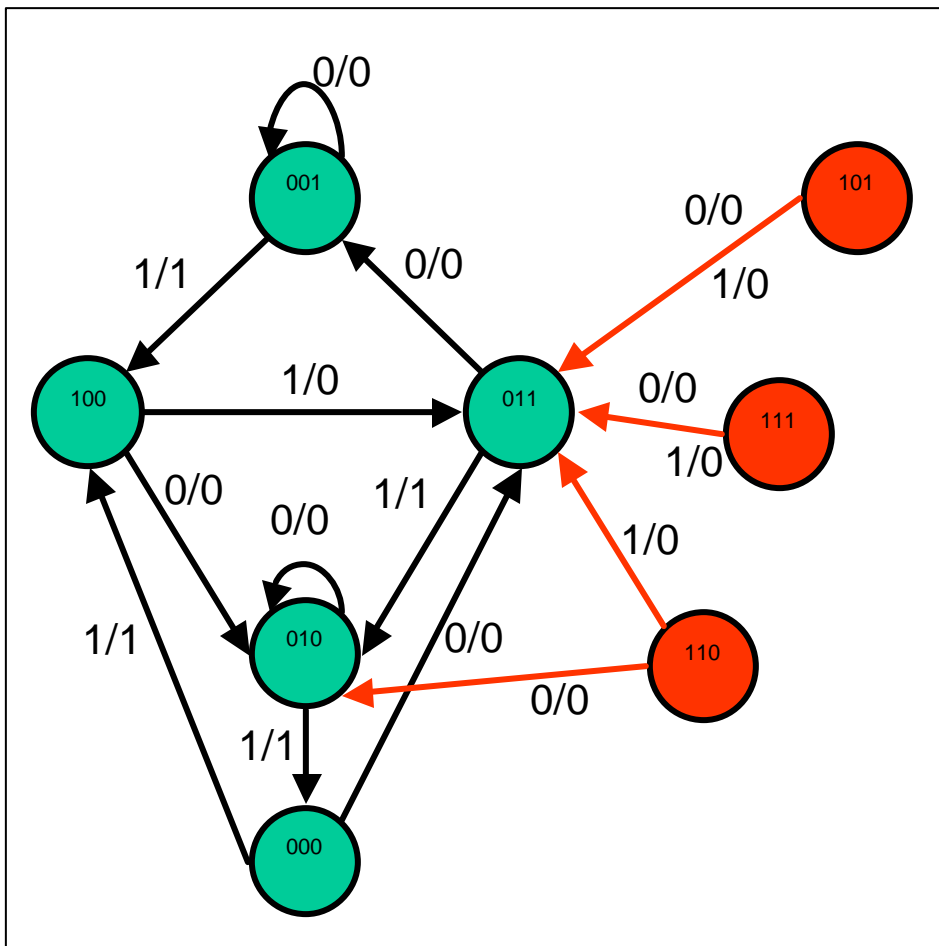
$$D_C = xA + x'C + x'A'B'$$

xA\BC	00	01	11	10
00	0	0	0	0
01	0	X0	X0	X0
11	0	X0	X0	X0
10	1	1	1	1

$$y = x'A$$

X1 indicates a don't care that has been set to 1
 X0 indicates a don't care that has been set to 0
 Resulting extra states:

State			Input	Next state			Output
A	B	C	x	A	B	C	y
1	0	1	0	0	1	1	0
1	0	1	1	0	1	1	0
1	1	0	0	0	1	0	0
1	1	0	1	0	1	1	0
1	1	1	0	0	1	1	0
1	1	1	1	0	1	1	0



b) with JK FF

State			Input	Next state			Output	Controls					
A	B	C	x	A	B	C	y	J _A	K _A	J _B	K _B	J _C	K _C
0	0	1	0	0	0	1	0	0	X	0	X	X	0
0	0	1	1	1	0	0	1	1	X	0	X	X	1
1	0	0	0	0	1	0	0	X	1	1	X	0	X
1	0	0	1	0	1	1	0	X	1	1	X	1	X
0	1	0	0	0	1	0	0	0	X	X	0	0	X
0	1	0	1	0	0	0	1	0	X	X	1	0	X
0	1	1	0	0	0	1	0	0	X	X	1	X	0
0	1	1	1	0	1	0	1	0	X	X	0	X	1
0	0	0	0	0	1	1	0	0	X	1	X	1	X
0	0	0	1	1	0	0	1	1	X	0	X	0	X

Q(t)	J	K	Q(t+1)
0	0	X	0
0	1	X	1
1	X	1	0
1	X	0	1

xA\BC	00	01	11	10
00	0	0	0	0
01	X0	X0	X0	X0
11	X1	X1	X0	X0
10	1	1	0	0

$$J_A = xB'$$

xA\BC	00	01	11	10
00	X1	X1	X1	X1
01	1	X1	X1	X1
11	1	X1	X1	X1
10	X1	X1	X1	X1

$$K_A = 1$$

xA\BC	00	01	11	10
00	1	0	X0	X1
01	1	X1	X1	X1
11	1	X1	X1	X1
10	0	0	X0	X0

$$J_B = A + x'C'$$

xA\BC	00	01	11	10
00	X0	X1	1	0
01	X0	X1	X1	X0
11	X1	X0	X0	X1
10	X1	X0	0	1

$$K_B = x'C + xC'$$

xA\BC	00	01	11	10
00	1	X1	X0	0
01	0	X0	X0	X0
11	1	X1	X1	X1
10	0	X0	X0	0

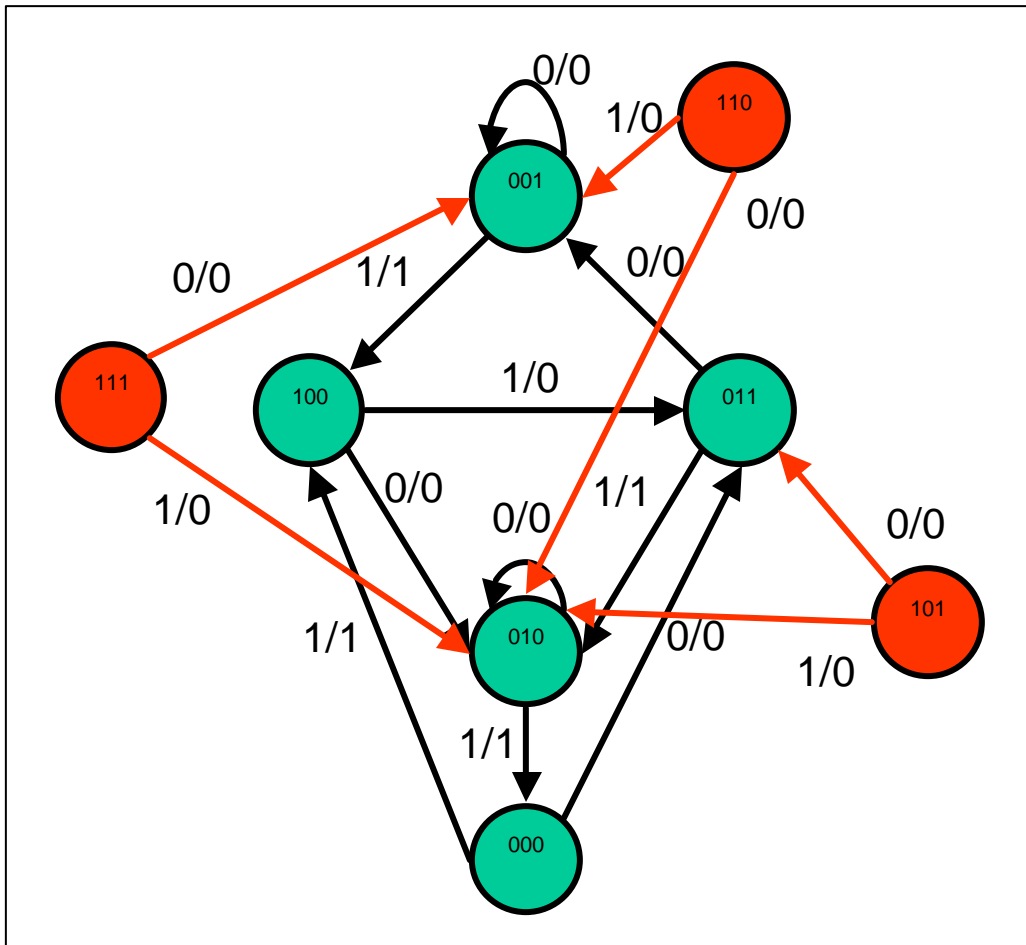
$$J_C = x'A'B' + xA$$

x\ABC	00	01	11	10
00	X0	0	0	X0
01	X0	X0	X0	X0
11	X1	X1	X1	X1
10	X1	1	1	X1

$$K_C = x$$

Resulting extra states:

State			Input	Next state			Output
A	B	C	x	A	B	C	y
1	0	1	0	0	1	1	0
1	0	1	1	0	1	0	0
1	1	0	0	0	1	0	0
1	1	0	1	0	0	1	0
1	1	1	0	0	0	1	0
1	1	1	1	0	1	0	0



6-4) The contents of a 4-bit register is initially 1101. The register is shifted six times to the right with the serial input being 101101. What is the content of the register after each shift?

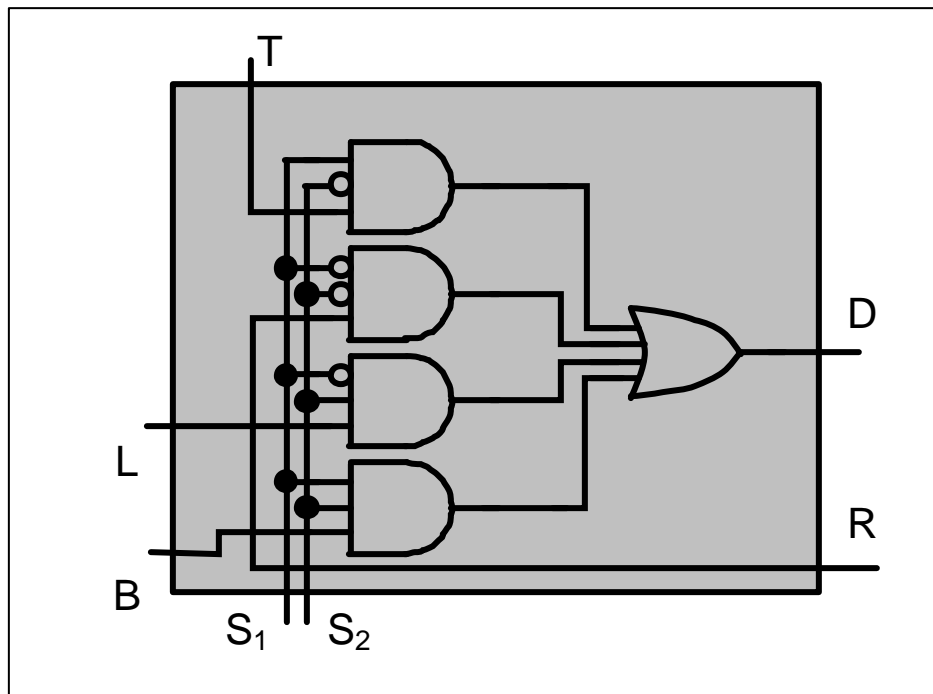
Register contents	Remaining input
1101	101101
1110	01101
0111	1101
1011	101
1101	01
0110	1
1011	-

Design a 3-bit Universal Shift Register using AND, OR, NOT, NAND or NOR gates and D Flip-flops that implements the following functions :

S ₁	S ₂	Function
0	0	Shift left
0	1	Shift right
1	0	Parallel load from top
1	1	Parallel load from bottom

The shift register has top and bottom D inputs and Q outputs, as well as right and left shift-in inputs and shift-out outputs

This is the Select logic at the input of each D FF:



This is the overall register design:

