CpE358/CS381

Switching Theory and Logical Design

Class 9

Today

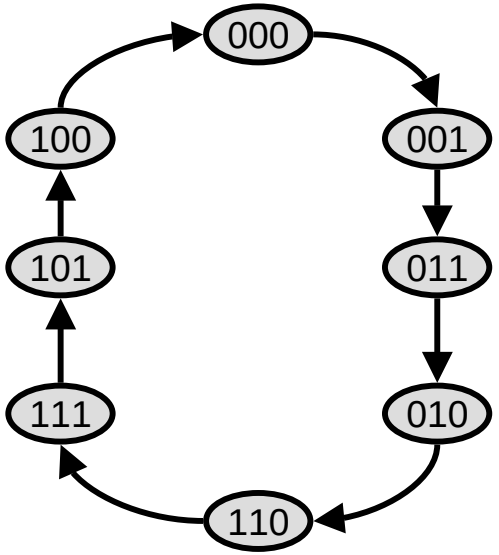
- Fundamental concepts of digital systems (Mano Chapter 1)
- Binary codes, number systems, and arithmetic (Ch 1)
- Boolean algebra (Ch 2)
- Simplification of switching equations (Ch 3)
- Digital device characteristics (e.g., TTL, CMOS)/design considerations (Ch 10)
- Combinatoric logical design including LSI implementation (Chapter 4)
- Flip-flops and state memory elements (Ch 5)
- Sequential logic analysis and design (Ch 5)
- Counters, shift register circuits (Ch 6)
- Hazards, Races, and time related issues in digital design (Ch 9)
- Synchronous vs. asynchronous design (Ch 9)
- Memory and Programmable logic (Ch 7)
- Minimization of sequential systems
- Introduction to Finite Automata

A slightly more complicated sequential design

- System description:
  - Design a circuit that transitions between states in Gray-code order (000,001,011,010,110,111,101,100,…) using J-K flip-flops

A slightly more complicated sequential design

- System description:
  - Design a circuit that transitions between states in Gray-code order (000,001,011,010,110,111,101,100,…) using J-K flip-flops
- State diagram:

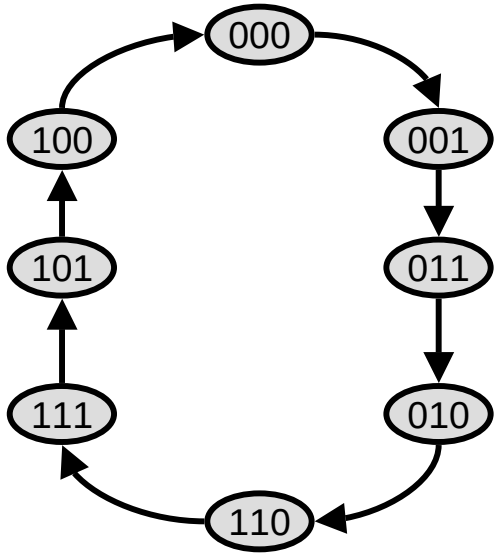


- All states are used, so 3 FFs are needed

A slightly more complicated sequential design

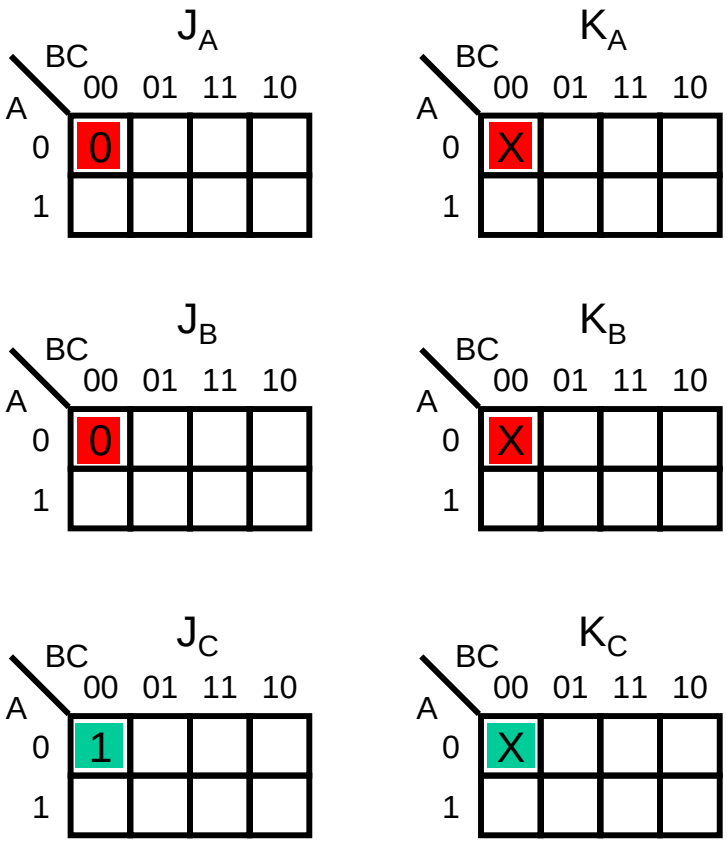
- State table:

Present State	Next State
000	001
001	011
010	110
011	010
100	000
101	100
110	111
111	101

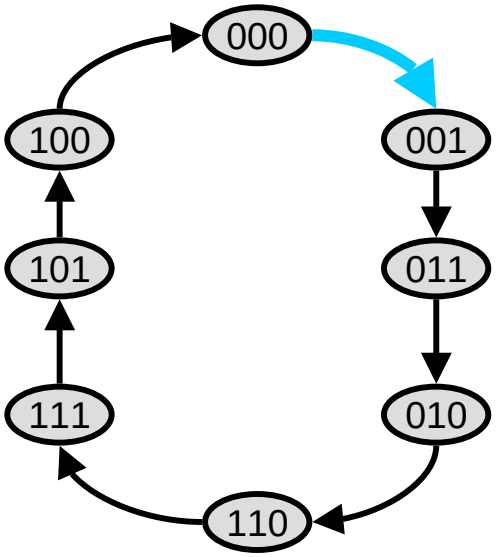


A slightly more complicated sequential design

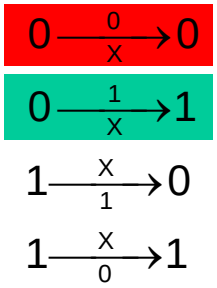
- Input functions for J-K



Present State	Next State
000	001
001	011
010	110
011	010
100	000
101	100
110	111
111	101



J-K operation:



A slightly more complicated sequential design

- Input functions for J-K

J_A

A \ BC	00	01	11	10
0	0	0	0	1
1	X	X	X	X

K_A

A \ BC	00	01	11	10
0	X	X	X	X
1	1	0	0	0

J_B

A \ BC	00	01	11	10
0	0	1	X	X
1	0	0	X	X

K_B

A \ BC	00	01	11	10
0	X	X	0	0
1	X	X	1	0

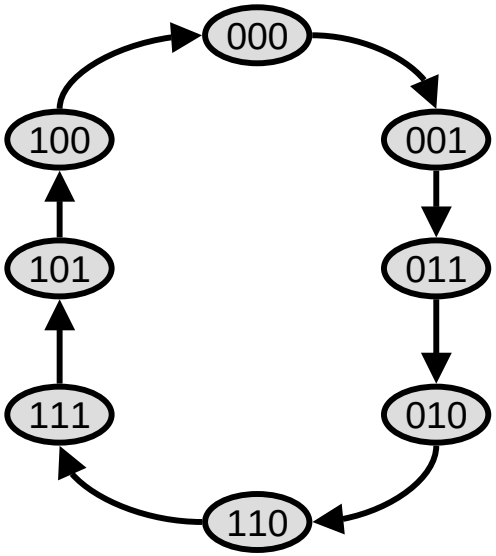
J_C

A \ BC	00	01	11	10
0	1	X	X	0
1	0	X	X	1

K_C

A \ BC	00	01	11	10
0	X	0	1	X
1	X	1	0	X

Present State	Next State
000	001
001	011
010	110
011	010
100	000
101	100
110	111
111	101



J-K operation:

$0 \xrightarrow[X]{0} 0$

$0 \xrightarrow[X]{1} 1$

$1 \xrightarrow[1]{X} 0$

$1 \xrightarrow[0]{X} 1$

A slightly more complicated sequential design

- Input functions for J-K

J_A

A \ BC	00	01	11	10
0	0	0	0	1
1	X	X	X	X

K_A

A \ BC	00	01	11	10
0	X	X	X	X
1	1	0	0	0

J_B

A \ BC	00	01	11	10
0	0	1	X	X
1	0	0	X	X

K_B

A \ BC	00	01	11	10
0	X	X	0	0
1	X	X	1	0

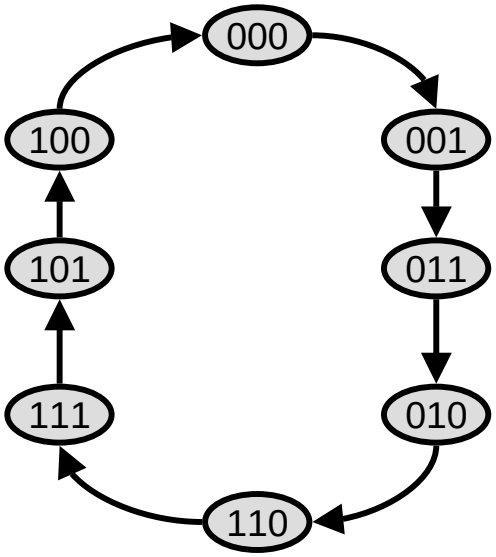
J_C

A \ BC	00	01	11	10
0	1	X	X	0
1	0	X	X	1

K_C

A \ BC	00	01	11	10
0	X	0	1	X
1	X	1	0	X

Present State	Next State
000	001
001	011
010	110
011	010
100	000
101	100
110	111
111	101



J-K operation:

$0 \xrightarrow[X]{0} 0$

$0 \xrightarrow[X]{1} 1$

$1 \xrightarrow[1]{X} 0$

$1 \xrightarrow[0]{X} 1$

A slightly more complicated sequential design

- Input functions for J-K

$J_A = BC'$

A \ BC	00	01	11	10
0	0	0	0	1
1	X	X	X	X

$K_A = B'C'$

A \ BC	00	01	11	10
0	X	X	X	X
1	1	0	0	0

$J_B = A'C$

A \ BC	00	01	11	10
0	0	1	X	X
1	0	0	X	X

$K_B = AC$

A \ BC	00	01	11	10
0	X	X	0	0
1	X	X	1	0

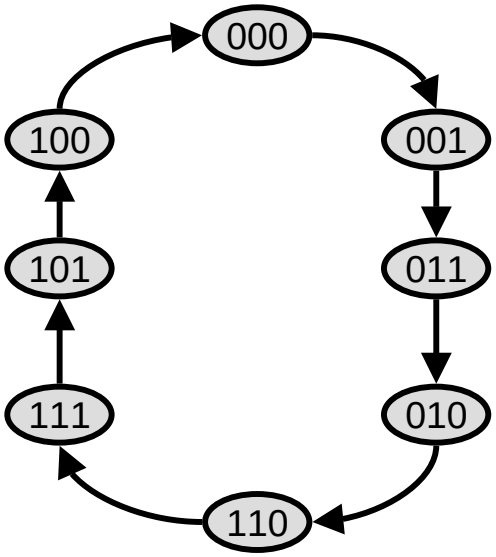
$J_C = A'B'+AB$

A \ BC	00	01	11	10
0	1	X	X	0
1	0	X	X	1

$K_C = AB'+A'B$

A \ BC	00	01	11	10
0	X	0	1	X
1	X	1	0	X

Present State	Next State
000	001
001	011
010	110
011	010
100	000
101	100
110	111
111	101



J-K operation:

$0 \xrightarrow{\substack{0 \\ X}} 0$

$0 \xrightarrow{\substack{1 \\ X}} 1$

$1 \xrightarrow{\substack{X \\ 1}} 0$

$1 \xrightarrow{\substack{X \\ 0}} 1$

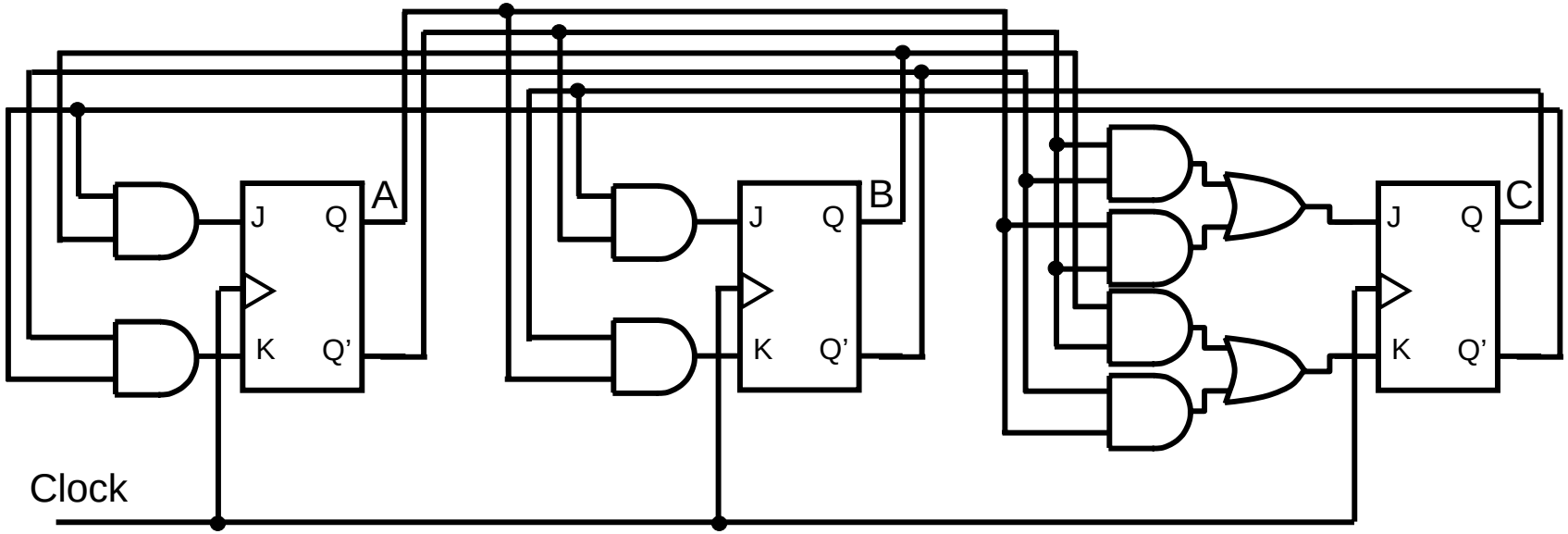
A slightly more complicated sequential design

- Input functions for J-K

$J_A = BC'$ $J_B = A'C$ $J_C = A'B' + AB$

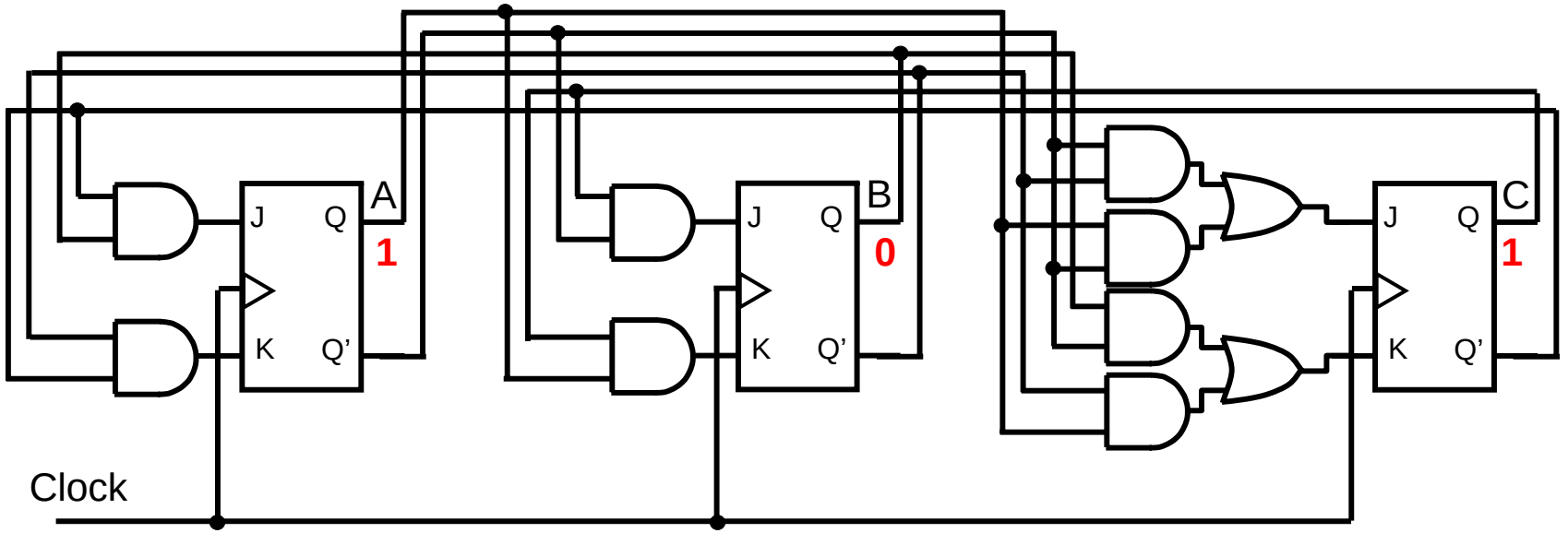
$K_A = B'C'$ $K_B = AC$ $K_C = AB' + A'B$

- Logic Diagram:



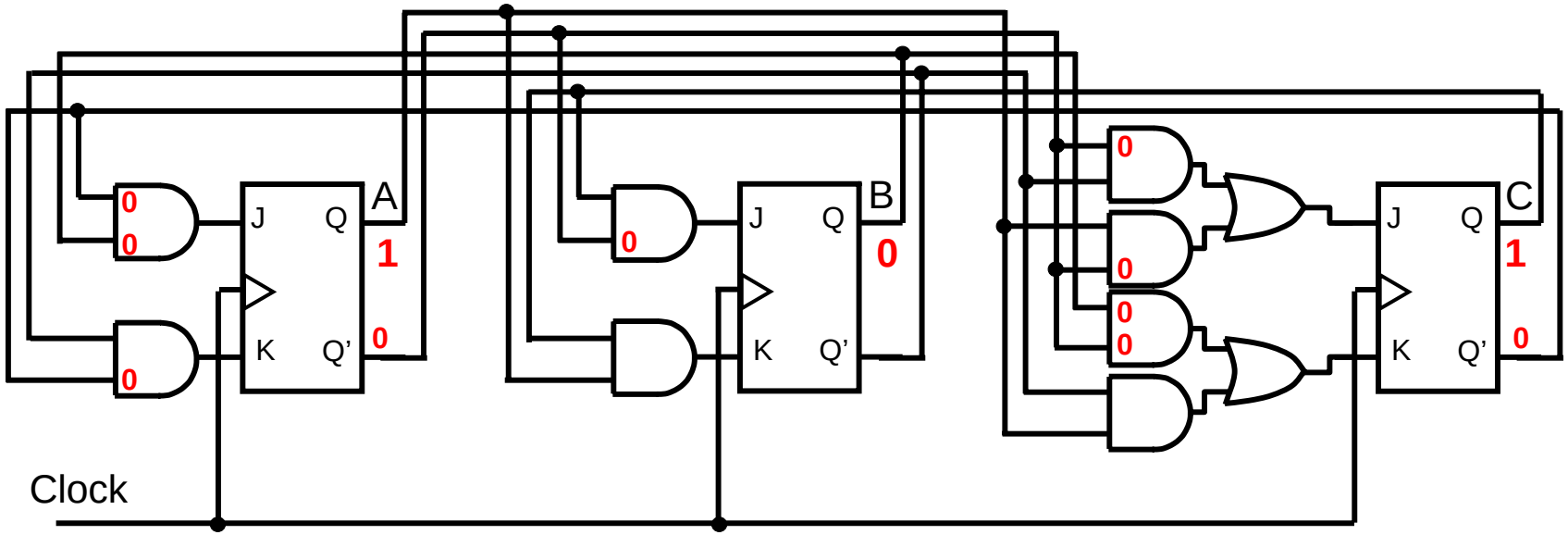
A slightly more complicated sequential design

- Verify correctness of logic diagram:



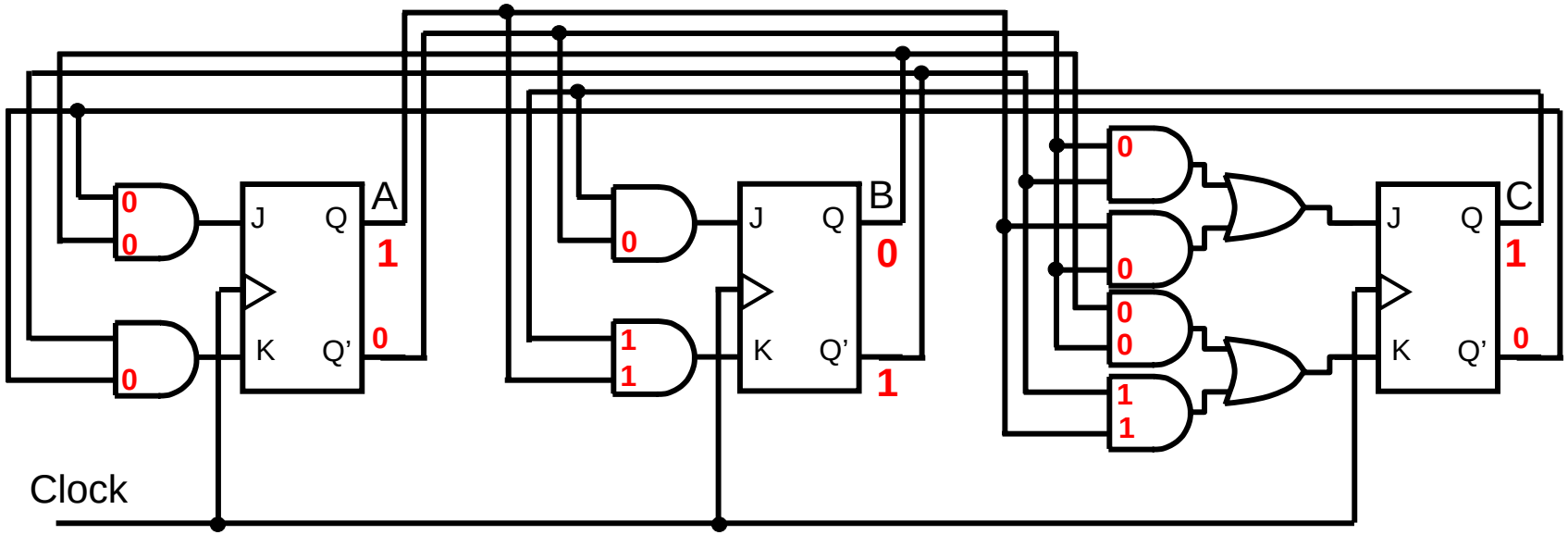
A slightly more complicated sequential design

- Verify correctness of logic diagram:



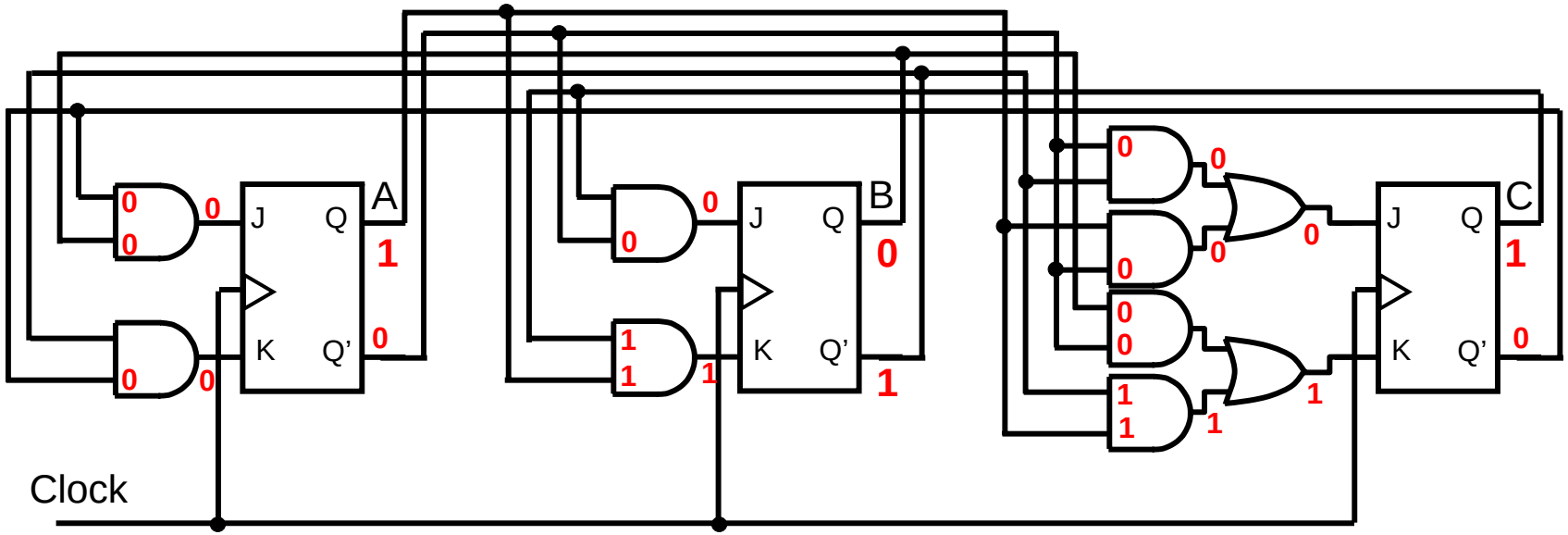
A slightly more complicated sequential design

- Verify correctness of logic diagram:



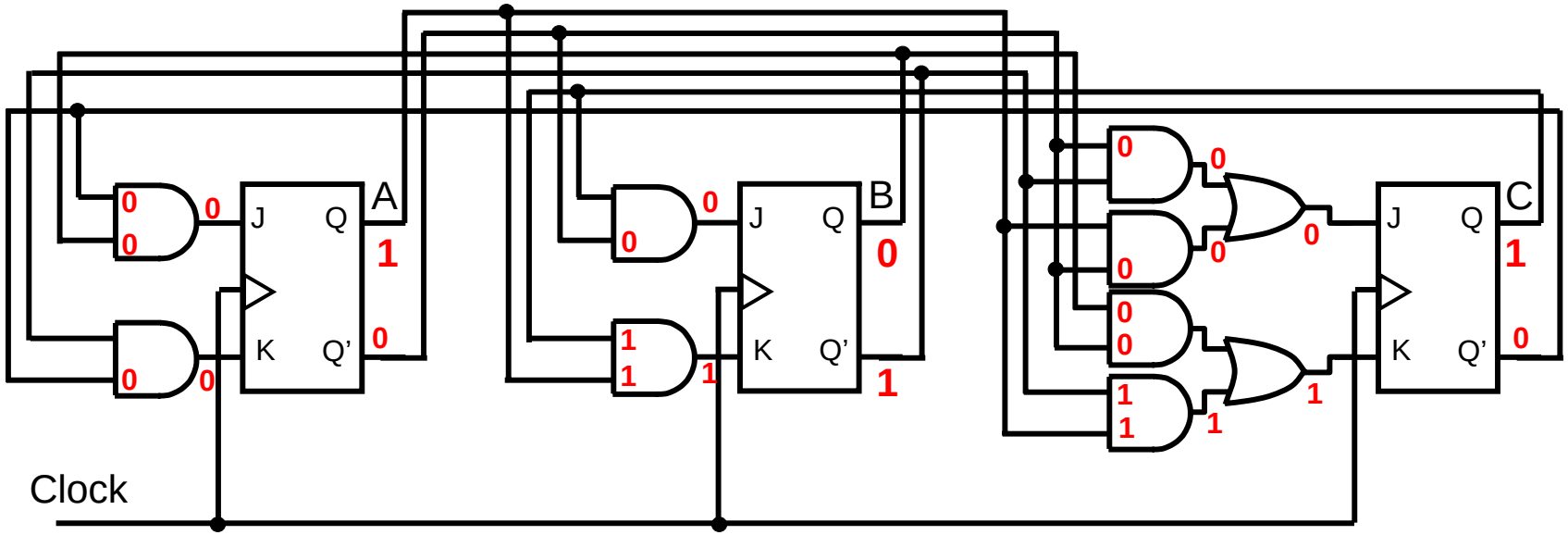
A slightly more complicated sequential design

- Verify correctness of logic diagram:



A slightly more complicated sequential design

- Verify correctness of logic diagram:

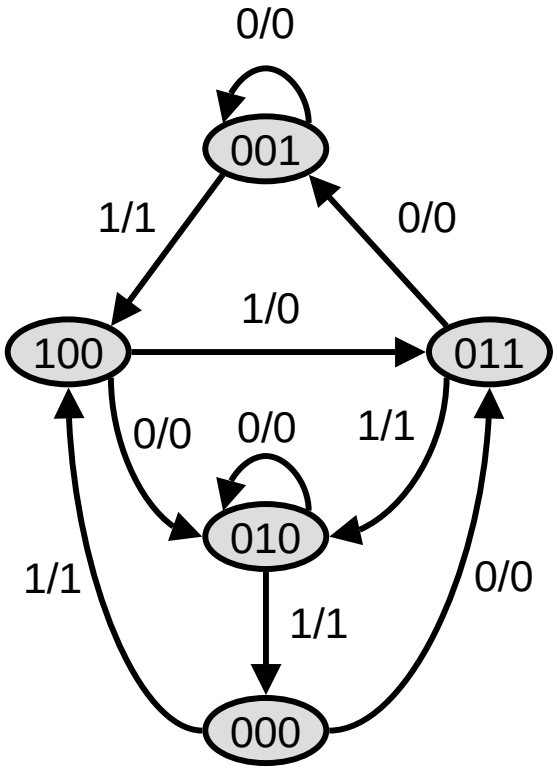


$1 \xrightarrow[0]{0} 1$ $\quad 0 \xrightarrow[1]{0} 0$ $\quad 1 \xrightarrow[1]{0} 0$

$101 \longrightarrow 100$

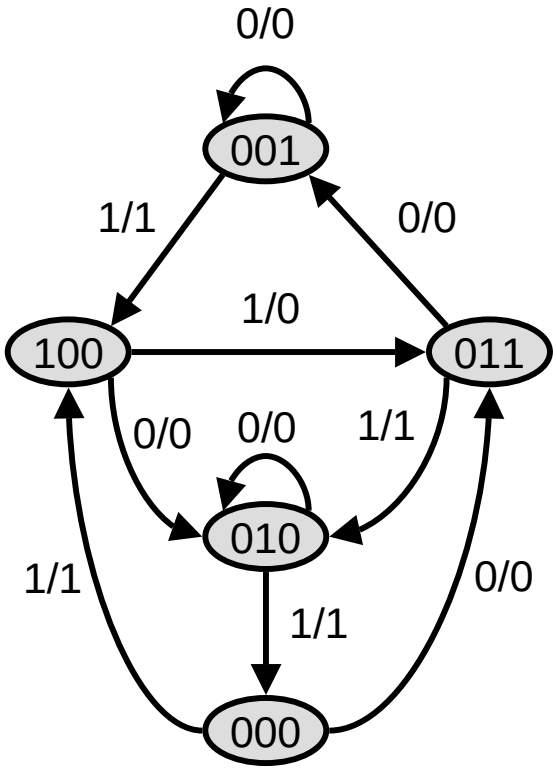
Problem 5-20

- Design a sequential circuit specified by the state diagram below using T flip-flops



Problem 5-20

- Design a sequential circuit specified by the state diagram below using T flip-flops

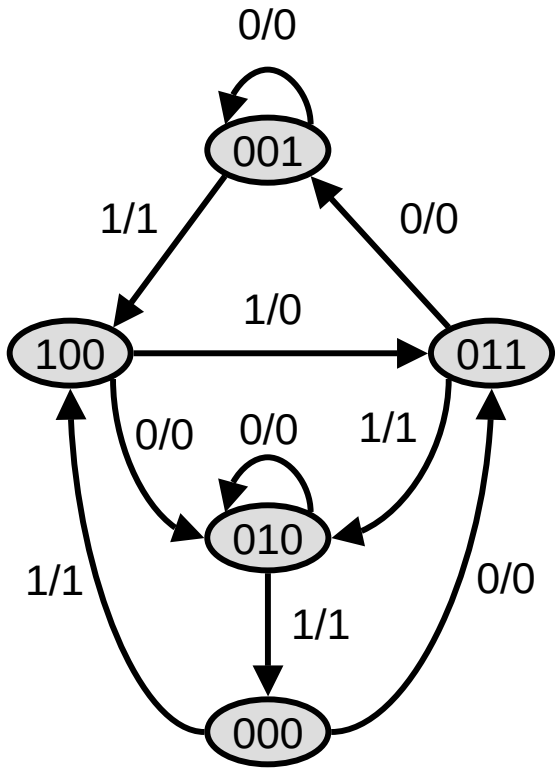


- 5 states -> 3 FFs will be needed

Problem 5-20

- Create the state table:

Present State	Input	Next State	Output
000	0	011	0
000	1	100	1
001	0	001	0
001	1	100	1
010	0	010	0
010	1	000	1
011	0	001	0
011	1	010	1
100	0	010	0
100	1	011	0



Problem 5-20

- Switching characteristics of a T FF:

$0 \xrightarrow{0} 0$

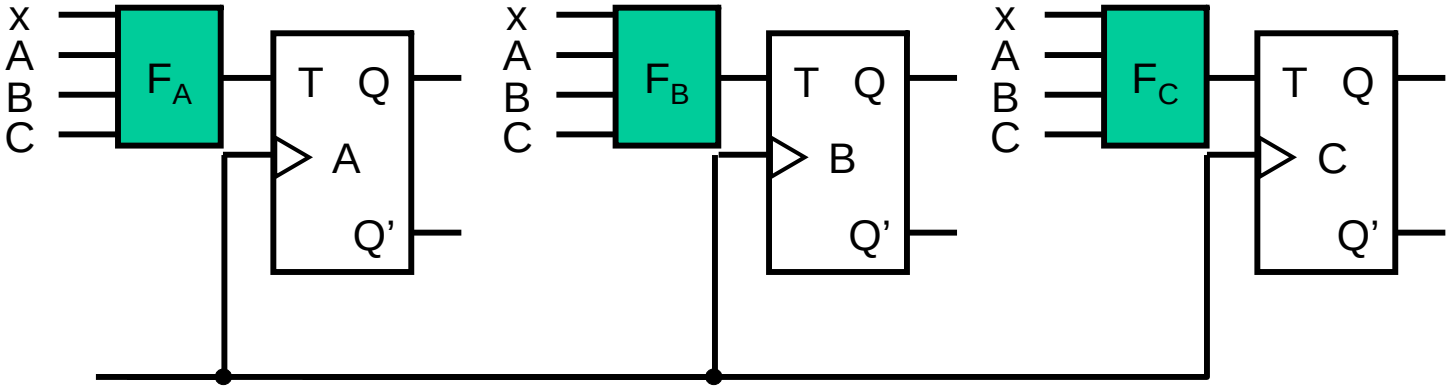
$0 \xrightarrow{1} 1$

$1 \xrightarrow{1} 0$

$1 \xrightarrow{0} 1$

- Derive input functions for FFs:

Present State	Input x	Next State	Output
000	0	011	0
000	1	100	1
001	0	001	0
001	1	100	1
010	0	010	0
010	1	000	1
011	0	001	0
011	1	010	1
100	0	010	0
100	1	011	0



Problem 5-20

Present State	Input x	Next State	Output
000	0	011	0
000	1	100	1
001	0	001	0
001	1	100	1
010	0	010	0
010	1	000	1
011	0	001	0
011	1	010	1
100	0	010	0
100	1	011	0

- Input functions for FFs:

A	B	C	Input x		
0	0	0	0		
0	0	0	1		
0	0	1	0		
0	0	1	1		
0	1	0	0		
0	1	0	1		
0	1	1	0		
0	1	1	1		
1	0	0	0		
1	0	0	1		

A	B	C	Input x		
0	0	0	0		
0	0	0	1		
0	0	1	0		
0	0	1	1		
0	1	0	0		
0	1	0	1		
0	1	1	0		
0	1	1	1		
1	0	0	0		
1	0	0	1		

A	B	C	Input x		
0	0	0	0		
0	0	0	1		
0	0	1	0		
0	0	1	1		
0	1	0	0		
0	1	0	1		
0	1	1	0		
0	1	1	1		
1	0	0	0		
1	0	0	1		

Problem 5-20

- Input functions for FFs:

Present State	Input x	Next State	Output
000	0	011	0
000	1	100	1
001	0	001	0
001	1	100	1
010	0	010	0
010	1	000	1
011	0	001	0
011	1	010	1
100	0	010	0
100	1	011	0

A	B	C	Input x	Next A	
0	0	0	0	0	
0	0	0	1	1	
0	0	1	0	0	
0	0	1	1	1	
0	1	0	0	0	
0	1	0	1	0	
0	1	1	0	0	
0	1	1	1	0	
1	0	0	0	0	
1	0	0	1	0	

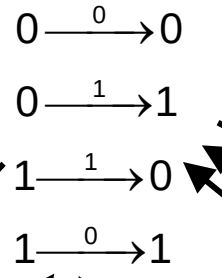
A	B	C	Input x	Next B	
0	0	0	0	1	
0	0	0	1	0	
0	0	1	0	0	
0	0	1	1	0	
0	1	0	0	1	
0	1	0	1	0	
0	1	1	0	0	
0	1	1	1	1	
1	0	0	0	1	
1	0	0	1	1	

A	B	C	Input x	Next C	
0	0	0	0	1	
0	0	0	1	0	
0	0	1	0	1	
0	0	1	1	0	
0	1	0	0	0	
0	1	0	1	0	
0	1	1	0	1	
0	1	1	1	0	
1	0	0	0	0	
1	0	0	1	1	

Problem 5-20

Present State	Input x	Next State	Output
000	0	011	0
000	1	100	1
001	0	001	0
001	1	100	1
010	0	010	0
010	1	000	1
011	0	001	0
011	1	010	1
100	0	010	0
100	1	011	0

- Input functions for FFs:



A	B	C	Input x	Next A	T_A
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	0	0
0	0	1	1	1	1
0	1	0	0	0	0
0	1	0	1	0	0
0	1	1	0	0	0
0	1	1	1	0	0
1	0	0	0	0	1
1	0	0	1	0	1

A	B	C	Input x	Next B	T_B
0	0	0	0	1	1
0	0	0	1	0	0
0	0	1	0	0	0
0	0	1	1	0	0
0	1	0	0	1	0
0	1	0	1	0	1
0	1	1	0	0	1
0	1	1	1	1	0
1	0	0	0	1	1
1	0	0	1	1	1

A	B	C	Input x	Next C	T_C
0	0	0	0	1	1
0	0	0	1	0	0
0	0	1	0	1	1
0	0	1	1	0	0
0	1	0	0	0	0
0	1	0	1	0	0
0	1	1	0	1	1
0	1	1	1	0	0
1	0	0	0	0	1
1	0	0	1	1	0

Problem 5-20

- Input functions for FFs:

Present State	Input x	Next State	Output
000	0	011	0
000	1	100	1
001	0	001	0
001	1	100	1
010	0	010	0
010	1	000	1
011	0	001	0
011	1	010	1
100	0	010	0
100	1	011	0

A	B	C	Input x	Next A	T_A
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	0	0
0	0	1	1	1	1
0	1	0	0	0	0
0	1	0	1	0	0
0	1	1	0	0	0
0	1	1	1	0	0
1	0	0	0	0	1
1	0	0	1	0	1

A	B	C	Input x	Next B	T_B
0	0	0	0	1	1
0	0	0	1	0	0
0	0	1	0	0	0
0	0	1	1	0	0
0	1	0	0	1	0
0	1	0	1	0	1
0	1	1	0	0	1
0	1	1	1	1	0
1	0	0	0	1	1
1	0	0	1	1	1

A	B	C	Input x	Next C	T_C
0	0	0	0	1	1
0	0	0	1	0	0
0	0	1	0	1	1
0	0	1	1	0	0
0	1	0	0	0	0
0	1	0	1	0	0
0	1	1	0	1	1
0	1	1	1	0	0
1	0	0	0	0	1
1	0	0	1	1	0

Problem 5-20

A	B	C	Input x	Next A	T_A
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	0	0
0	0	1	1	1	1
0	1	0	0	0	0
0	1	0	1	0	0
0	1	1	0	0	0
0	1	1	1	0	0
1	0	0	0	0	1
1	0	0	1	0	1

A	B	C	Input x	Next B	T_B
0	0	0	0	1	1
0	0	0	1	0	0
0	0	1	0	0	0
0	0	1	1	0	0
0	1	0	0	1	0
0	1	0	1	0	1
0	1	1	0	0	1
0	1	1	1	1	0
1	0	0	0	1	1
1	0	0	1	1	1

A	B	C	Input x	Next C	T_C
0	0	0	0	1	1
0	0	0	1	0	0
0	0	1	0	1	1
0	0	1	1	0	0
0	1	0	0	0	0
0	1	0	1	0	0
0	1	1	0	1	1
0	1	1	1	0	0
1	0	0	0	0	1
1	0	0	1	1	0

		BC			
		00	01	11	10
xA	00	0			
	01				
	11				
	10				

T_A

		BC			
		00	01	11	10
xA	00	1			
	01				
	11				
	10				

T_B

		BC			
		00	01	11	10
xA	00	1			
	01				
	11				
	10				

T_C

Problem 5-20

A	B	C	Input x	Next A	T_A
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	0	0
0	0	1	1	1	1
0	1	0	0	0	0
0	1	0	1	0	0
0	1	1	0	0	0
0	1	1	1	0	0
1	0	0	0	0	1
1	0	0	1	0	1

A	B	C	Input x	Next B	T_B
0	0	0	0	1	1
0	0	0	1	0	0
0	0	1	0	0	0
0	0	1	1	0	0
0	1	0	0	1	0
0	1	0	1	0	1
0	1	1	0	0	1
0	1	1	1	1	0
1	0	0	0	1	1
1	0	0	1	1	1

A	B	C	Input x	Next C	T_C
0	0	0	0	1	1
0	0	0	1	0	0
0	0	1	0	1	1
0	0	1	1	0	0
0	1	0	0	0	0
0	1	0	1	0	0
0	1	1	0	1	1
0	1	1	1	0	0
1	0	0	0	0	1
1	0	0	1	1	0

		BC			
		00	01	11	10
xA	00	0	0	0	0
	01	1			
	11	1			
	10	1	1	0	0

T_A

		BC			
		00	01	11	10
xA	00	1	0	1	0
	01	1			
	11	1			
	10	0	0	1	0

T_B

		BC			
		00	01	11	10
xA	00	1	1	1	0
	01	0			
	11	0			
	10	0	0	1	0

T_C

Problem 5-20

A	B	C	Input x	Next A	T_A
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	0	0
0	0	1	1	1	1
0	1	0	0	0	0
0	1	0	1	0	0
0	1	1	0	0	0
0	1	1	1	0	0
1	0	0	0	0	1
1	0	0	1	0	1

A	B	C	Input x	Next B	T_B
0	0	0	0	1	1
0	0	0	1	0	0
0	0	1	0	0	0
0	0	1	1	0	0
0	1	0	0	1	0
0	1	0	1	0	1
0	1	1	0	0	1
0	1	1	1	1	0
1	0	0	0	1	1
1	0	0	1	1	1

A	B	C	Input x	Next C	T_C
0	0	0	0	1	1
0	0	0	1	0	0
0	0	1	0	1	1
0	0	1	1	0	0
0	1	0	0	0	0
0	1	0	1	0	0
0	1	1	0	1	1
0	1	1	1	0	0
1	0	0	0	0	1
1	0	0	1	1	0

		BC			
		00	01	11	10
xA	00	0	0	0	0
	01	1	X	X	X
	11	1	X	X	X
	10	1	1	0	0

T_A

		BC			
		00	01	11	10
xA	00	1	0	1	0
	01	1	X	X	X
	11	1	X	X	X
	10	0	0	1	0

T_B

		BC			
		00	01	11	10
xA	00	1	1	1	0
	01	0	X	X	X
	11	0	X	X	X
	10	0	0	1	0

T_C

Problem 5-20

A	B	C	Input x	Next A	T_A
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	0	0
0	0	1	1	1	1
0	1	0	0	0	0
0	1	0	1	0	0
0	1	1	0	0	0
0	1	1	1	0	0
1	0	0	0	0	1
1	0	0	1	0	1

A	B	C	Input x	Next B	T_B
0	0	0	0	1	1
0	0	0	1	0	0
0	0	1	0	0	0
0	0	1	1	0	0
0	1	0	0	1	0
0	1	0	1	0	1
0	1	1	0	0	1
0	1	1	1	1	0
1	0	0	0	1	1
1	0	0	1	1	1

A	B	C	Input x	Next C	T_C
0	0	0	0	1	1
0	0	0	1	0	0
0	0	1	0	1	1
0	0	1	1	0	0
0	1	0	0	0	0
0	1	0	1	0	0
0	1	1	0	1	1
0	1	1	1	0	0
1	0	0	0	0	1
1	0	0	1	1	0

		BC			
		00	01	11	10
xA	00	0	0	0	0
	01	1	X	X	X
	11	1	X	X	X
	10	1	1	0	0

T_A

		BC			
		00	01	11	10
xA	00	1	0	1	0
	01	1	X	X	X
	11	1	X	X	X
	10	0	0	1	0

T_B

		BC			
		00	01	11	10
xA	00	1	1	1	0
	01	0	X	X	X
	11	0	X	X	X
	10	0	0	1	0

T_C

Problem 5-20

A	B	C	Input x	Next A	T_A
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	0	0
0	0	1	1	1	1
0	1	0	0	0	0
0	1	0	1	0	0
0	1	1	0	0	0
0	1	1	1	0	0
1	0	0	0	0	1
1	0	0	1	0	1

A	B	C	Input x	Next B	T_B
0	0	0	0	1	1
0	0	0	1	0	0
0	0	1	0	0	0
0	0	1	1	0	0
0	1	0	0	1	0
0	1	0	1	0	1
0	1	1	0	0	1
0	1	1	1	1	0
1	0	0	0	1	1
1	0	0	1	1	1

A	B	C	Input x	Next C	T_C
0	0	0	0	1	1
0	0	0	1	0	0
0	0	1	0	1	1
0	0	1	1	0	0
0	1	0	0	0	0
0	1	0	1	0	0
0	1	1	0	1	1
0	1	1	1	0	0
1	0	0	0	0	1
1	0	0	1	1	0

		BC			
		00	01	11	10
xA	00	0	0	0	0
	01	1	X	X	X
	11	1	X	X	X
	10	1	1	0	0

T_A

		BC			
		00	01	11	10
xA	00	1	0	1	0
	01	1	X	X	X
	11	1	X	X	X
	10	0	0	1	0

T_B

		BC			
		00	01	11	10
xA	00	1	1	1	0
	01	0	X	X	X
	11	0	X	X	X
	10	0	0	1	0

T_C

Problem 5-20

A	B	C	Input x	Next A	T_A
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	0	0
0	0	1	1	1	1
0	1	0	0	0	0
0	1	0	1	0	0
0	1	1	0	0	0
0	1	1	1	0	0
1	0	0	0	0	1
1	0	0	1	0	1

A	B	C	Input x	Next B	T_B
0	0	0	0	1	1
0	0	0	1	0	0
0	0	1	0	0	0
0	0	1	1	0	0
0	1	0	0	1	0
0	1	0	1	0	1
0	1	1	0	0	1
0	1	1	1	1	0
1	0	0	0	1	1
1	0	0	1	1	1

A	B	C	Input x	Next C	T_C
0	0	0	0	1	1
0	0	0	1	0	0
0	0	1	0	1	1
0	0	1	1	0	0
0	1	0	0	0	0
0	1	0	1	0	0
0	1	1	0	1	1
0	1	1	1	0	0
1	0	0	0	0	1
1	0	0	1	1	0

		BC			
		00	01	11	10
xA	00	0	0	0	0
	01	1	X	X	X
	11	1	X	X	X
	10	1	1	0	0

T_A

		BC			
		00	01	11	10
xA	00	1	0	1	0
	01	1	X	X	X
	11	1	X	X	X
	10	0	0	1	0

T_B

		BC			
		00	01	11	10
xA	00	1	1	1	0
	01	0	X	X	X
	11	0	X	X	X
	10	0	0	1	0

T_C

Problem 5-20

A	B	C	Input x	Next A	T_A
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	0	0
0	0	1	1	1	1
0	1	0	0	0	0
0	1	0	1	0	0
0	1	1	0	0	0
0	1	1	1	0	0
1	0	0	0	0	1
1	0	0	1	0	1

A	B	C	Input x	Next B	T_B
0	0	0	0	1	1
0	0	0	1	0	0
0	0	1	0	0	0
0	0	1	1	0	0
0	1	0	0	1	0
0	1	0	1	0	1
0	1	1	0	0	1
0	1	1	1	1	0
1	0	0	0	1	1
1	0	0	1	1	1

A	B	C	Input x	Next C	T_C
0	0	0	0	1	1
0	0	0	1	0	0
0	0	1	0	1	1
0	0	1	1	0	0
0	1	0	0	0	0
0	1	0	1	0	0
0	1	1	0	1	1
0	1	1	1	0	0
1	0	0	0	0	1
1	0	0	1	1	0

		BC			
		00	01	11	10
xA	00	0	0	0	0
	01	1	X	X	X
	11	1	X	X	X
	10	1	1	0	0

T_A

		BC			
		00	01	11	10
xA	00	1	0	1	0
	01	1	X	X	X
	11	1	X	X	X
	10	0	0	1	0

T_B

		BC			
		00	01	11	10
xA	00	1	1	1	0
	01	0	X	X	X
	11	0	X	X	X
	10	0	0	1	0

T_C

Problem 5-20

A	B	C	Input x	Next A	T_A
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	0	0
0	0	1	1	1	1
0	1	0	0	0	0
0	1	0	1	0	0
0	1	1	0	0	0
0	1	1	1	0	0
1	0	0	0	0	1
1	0	0	1	0	1

A	B	C	Input x	Next B	T_B
0	0	0	0	1	1
0	0	0	1	0	0
0	0	1	0	0	0
0	0	1	1	0	0
0	1	0	0	1	0
0	1	0	1	0	1
0	1	1	0	0	1
0	1	1	1	1	0
1	0	0	0	1	1
1	0	0	1	1	1

A	B	C	Input x	Next C	T_C
0	0	0	0	1	1
0	0	0	1	0	0
0	0	1	0	1	1
0	0	1	1	0	0
0	1	0	0	0	0
0	1	0	1	0	0
0	1	1	0	1	1
0	1	1	1	0	0
1	0	0	0	0	1
1	0	0	1	1	0

		BC			
		00	01	11	10
xA	00	0	0	0	0
	01	1	X	X	X
	11	1	X	X	X
	10	1	1	0	0

T_A

		BC			
		00	01	11	10
xA	00	1	0	1	0
	01	1	X	X	X
	11	1	X	X	X
	10	0	0	1	0

T_B

		BC			
		00	01	11	10
xA	00	1	1	1	0
	01	0	X	X	X
	11	0	X	X	X
	10	0	0	1	0

T_C

Problem 5-20

A	B	C	Input x	Next A	T_A
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	0	0
0	0	1	1	1	1
0	1	0	0	0	0
0	1	0	1	0	0
0	1	1	0	0	0
0	1	1	1	0	0
1	0	0	0	0	1
1	0	0	1	0	1

A	B	C	Input x	Next B	T_B
0	0	0	0	1	1
0	0	0	1	0	0
0	0	1	0	0	0
0	0	1	1	0	0
0	1	0	0	1	0
0	1	0	1	0	1
0	1	1	0	0	1
0	1	1	1	1	0
1	0	0	0	1	1
1	0	0	1	1	1

A	B	C	Input x	Next C	T_C
0	0	0	0	1	1
0	0	0	1	0	0
0	0	1	0	1	1
0	0	1	1	0	0
0	1	0	0	0	0
0	1	0	1	0	0
0	1	1	0	1	1
0	1	1	1	0	0
1	0	0	0	0	1
1	0	0	1	1	0

		BC			
		00	01	11	10
xA	00	0	0	0	0
	01	1	X	X	X
	11	1	X	X	X
	10	1	1	0	0

T_A

		BC			
		00	01	11	10
xA	00	1	0	1	0
	01	1	X	X	X
	11	1	X	X	X
	10	0	0	1	0

T_B

		BC			
		00	01	11	10
xA	00	1	1	1	0
	01	0	X	X	X
	11	0	X	X	X
	10	0	0	1	0

T_C

Problem 5-20

A	B	C	Input x	Next A	T_A
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	0	0
0	0	1	1	1	1
0	1	0	0	0	0
0	1	0	1	0	0
0	1	1	0	0	0
0	1	1	1	0	0
1	0	0	0	0	1
1	0	0	1	0	1

A	B	C	Input x	Next B	T_B
0	0	0	0	1	1
0	0	0	1	0	0
0	0	1	0	0	0
0	0	1	1	0	0
0	1	0	0	1	0
0	1	0	1	0	1
0	1	1	0	0	1
0	1	1	1	1	0
1	0	0	0	1	1
1	0	0	1	1	1

A	B	C	Input x	Next C	T_C
0	0	0	0	1	1
0	0	0	1	0	0
0	0	1	0	1	1
0	0	1	1	0	0
0	1	0	0	0	0
0	1	0	1	0	0
0	1	1	0	1	1
0	1	1	1	0	0
1	0	0	0	0	1
1	0	0	1	1	0

		BC			
		00	01	11	10
xA	00	0	0	0	0
	01	1	X	X	X
	11	1	X	X	X
	10	1	1	0	0

$T_A = A + xB'$

		BC			
		00	01	11	10
xA	00	1	0	1	0
	01	1	X	X	X
	11	1	X	X	X
	10	0	0	1	0

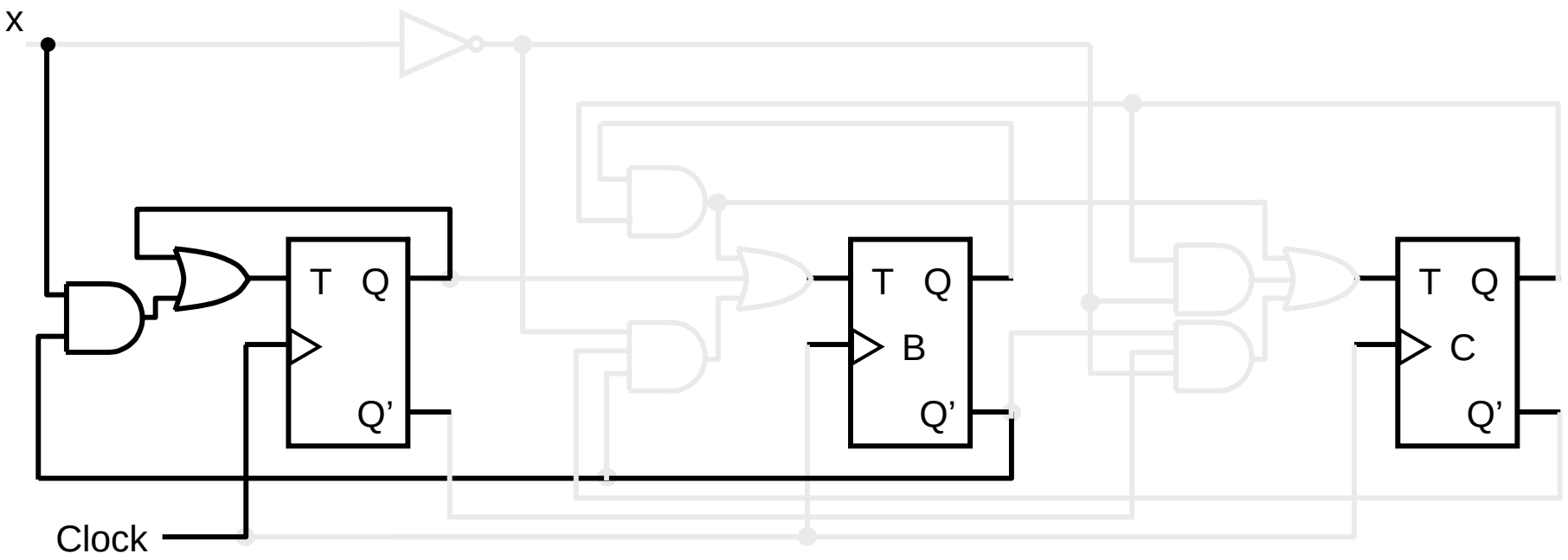
$T_B = A + BC + x'B'C'$

		BC			
		00	01	11	10
xA	00	1	1	1	0
	01	0	X	X	X
	11	0	X	X	X
	10	0	0	1	0

$T_C = BC + x'C + x'A'B'$

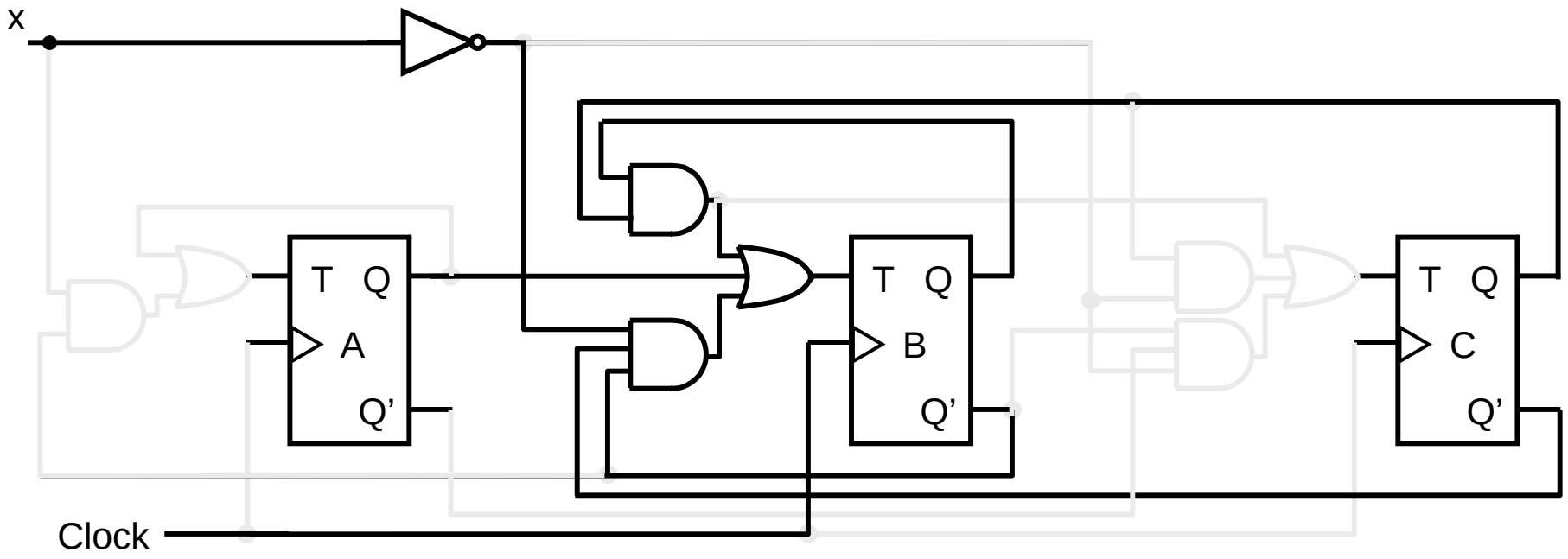
Problem 5-20

$T_A = A + xB'$ $T_B = A + BC + x'B'C'$ $T_C = BC + x'C + x'A'B'$



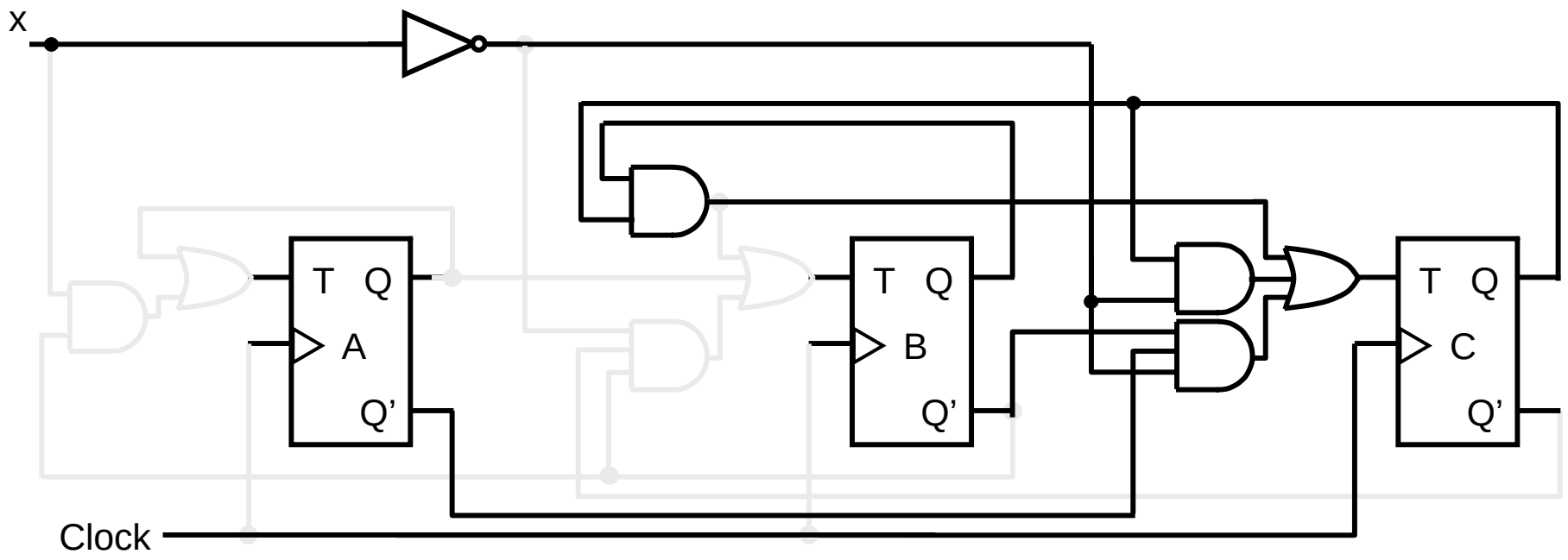
Problem 5-20

$T_B = A + BC + x'B'C'$



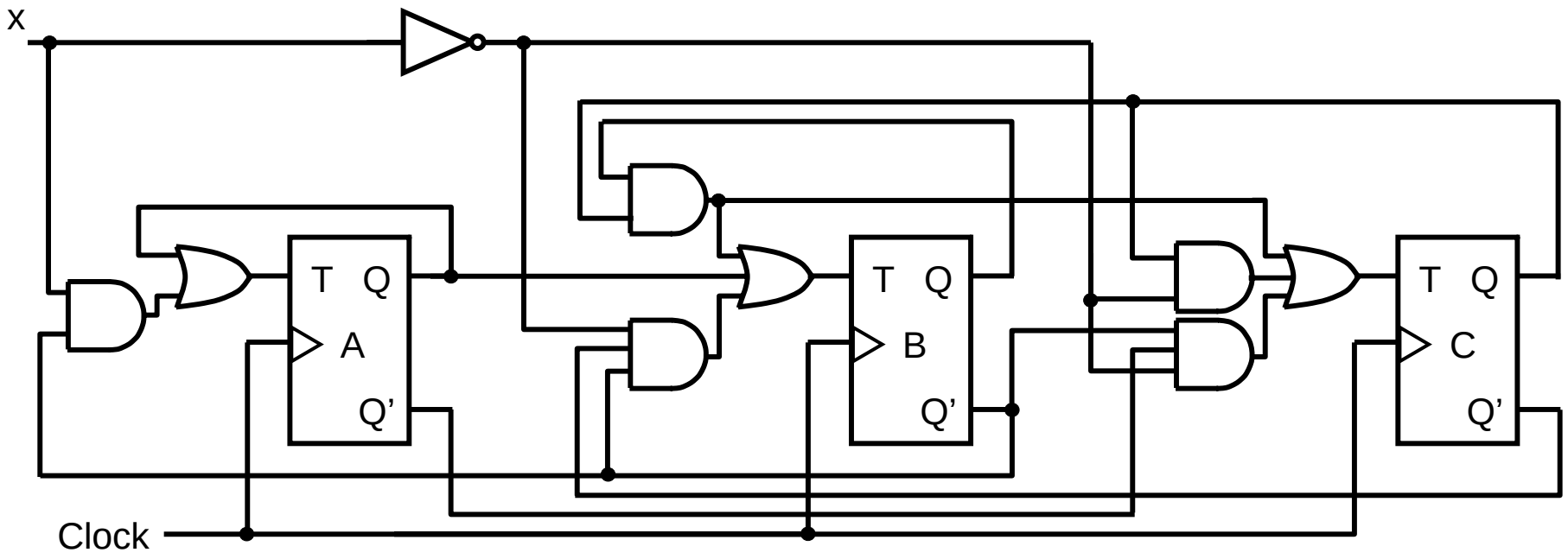
Problem 5-20

TA = A + xB’ TB = A + BC + x’B’C’ $T_C = BC + x'C + x'A'B'$

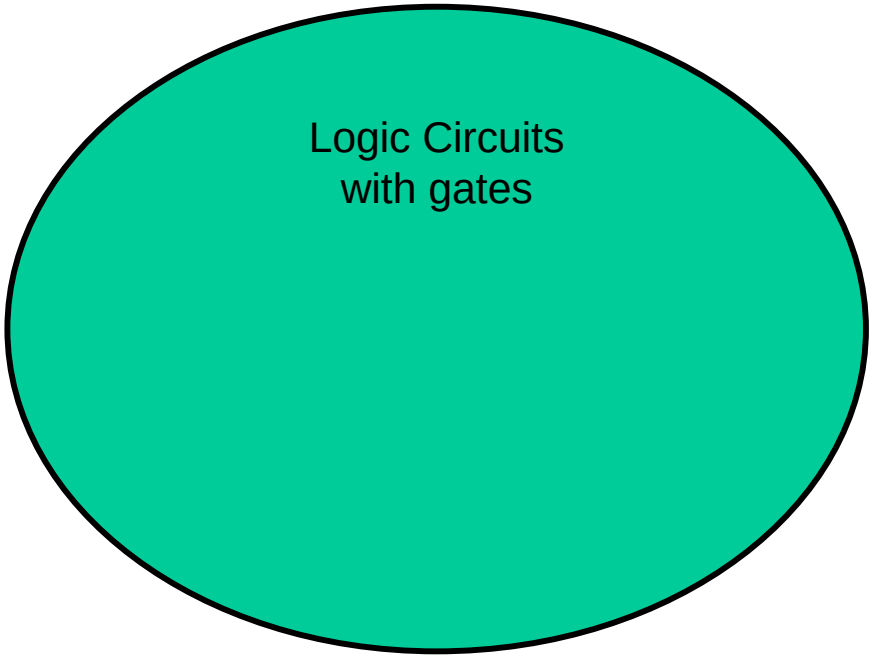


Problem 5-20

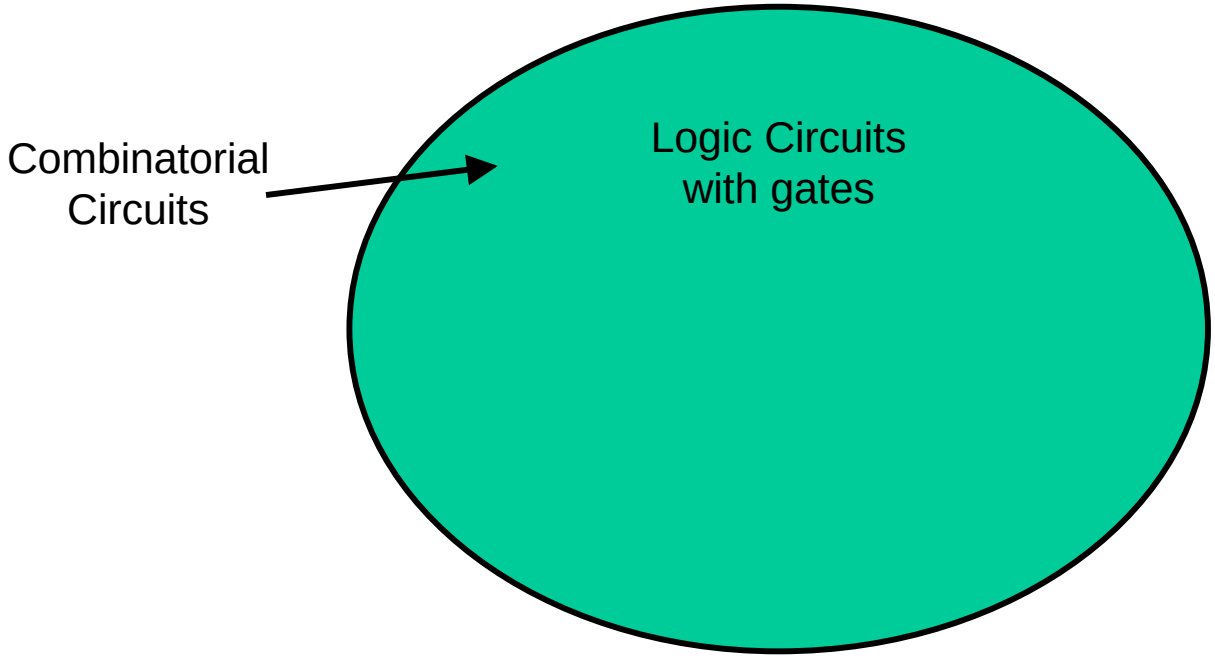
$T_A = A + xB'$ $T_B = A + BC + x'B'C'$ $T_C = BC + x'C + x'A'B'$



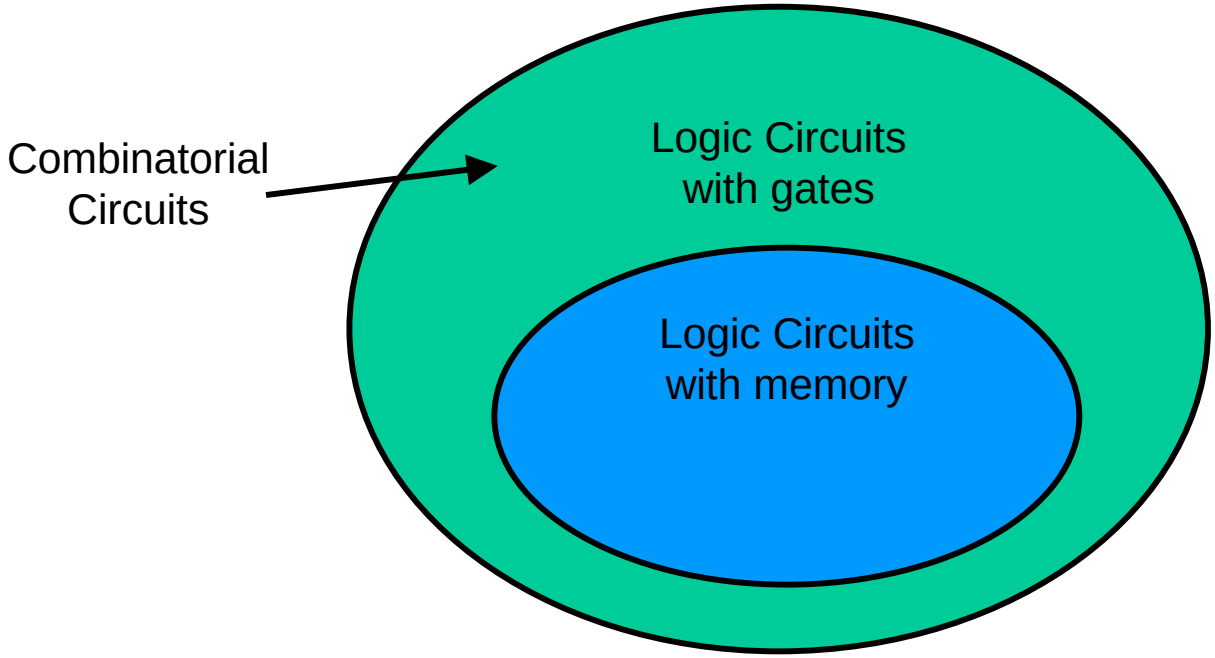
Course Roadmap



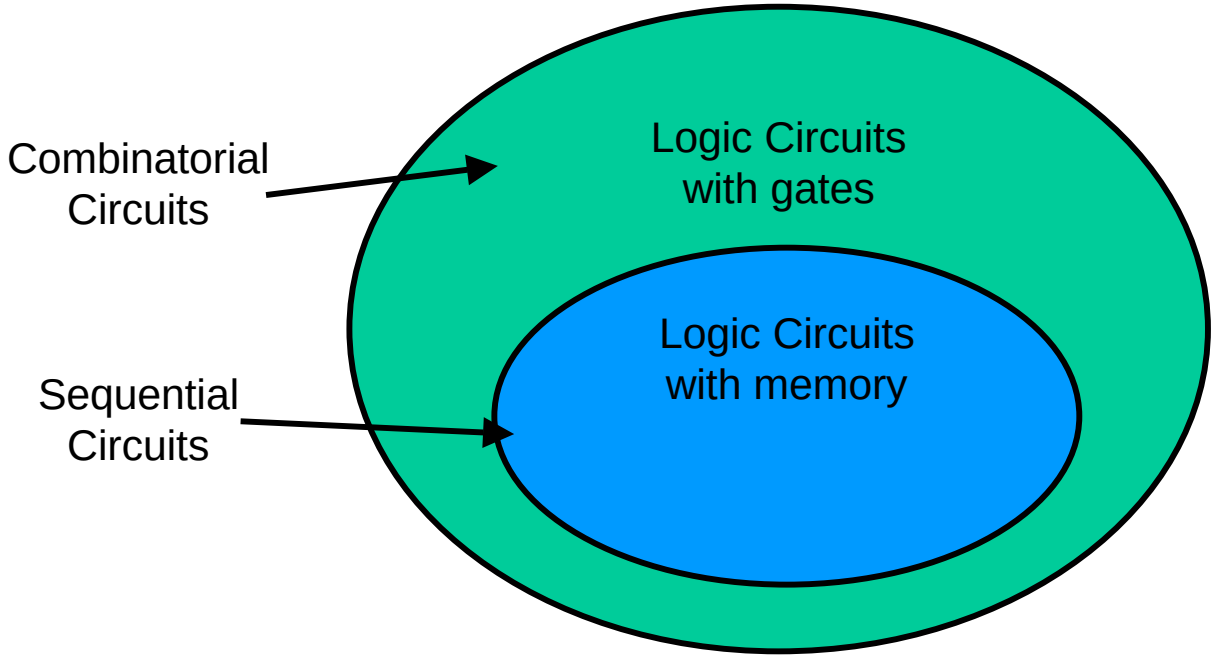
Course Roadmap



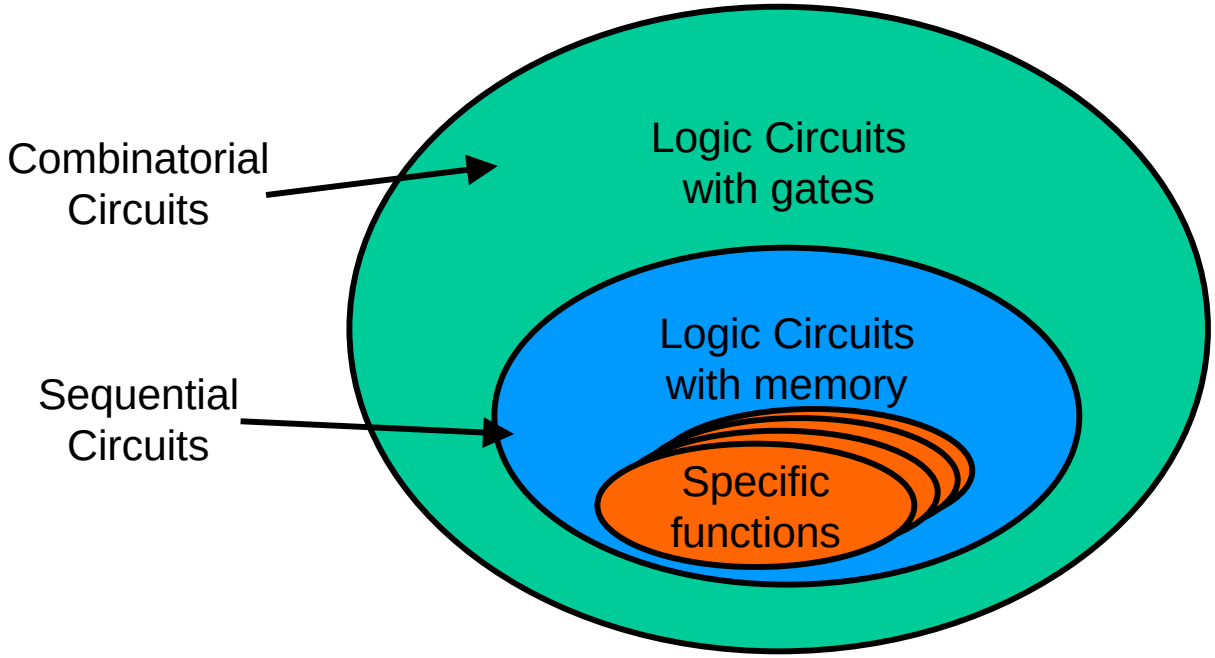
Course Roadmap



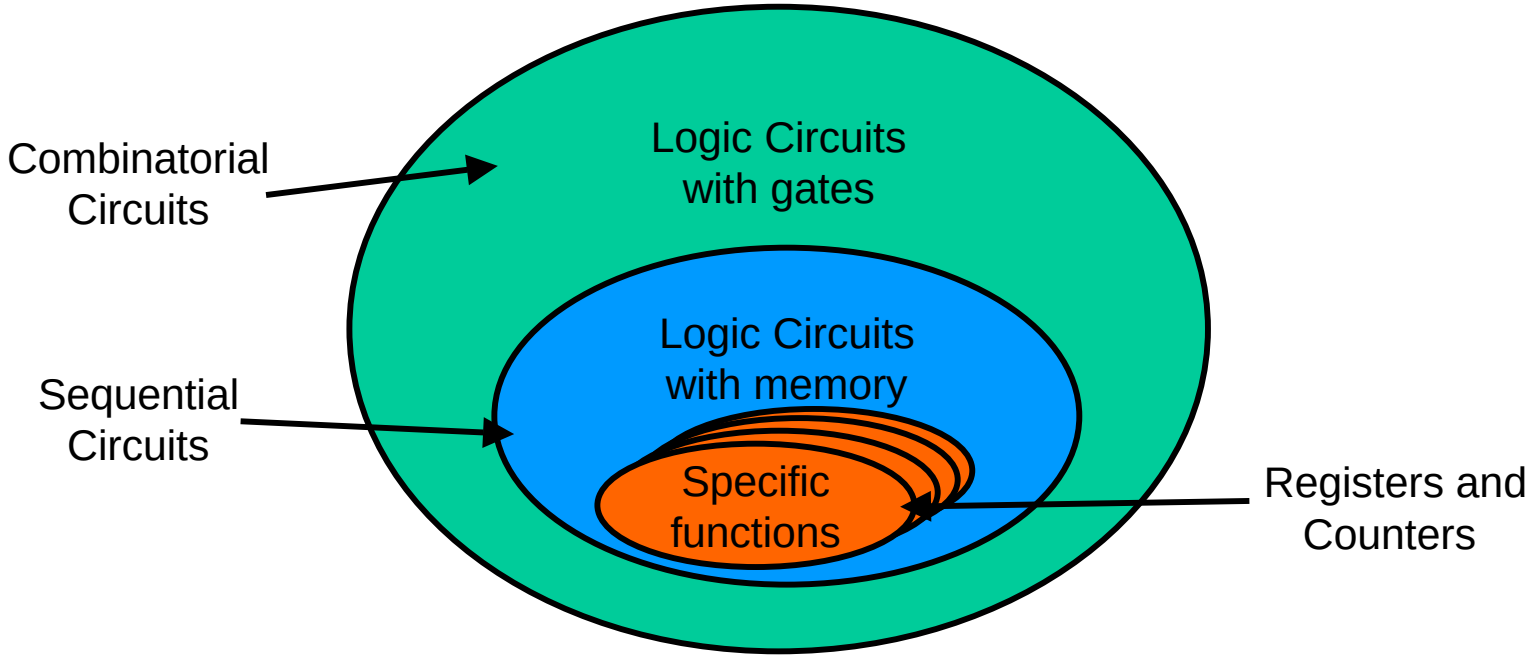
Course Roadmap



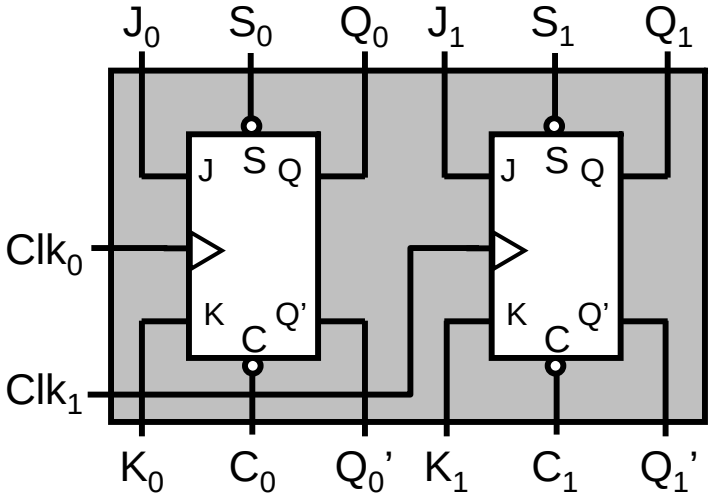
Course Roadmap

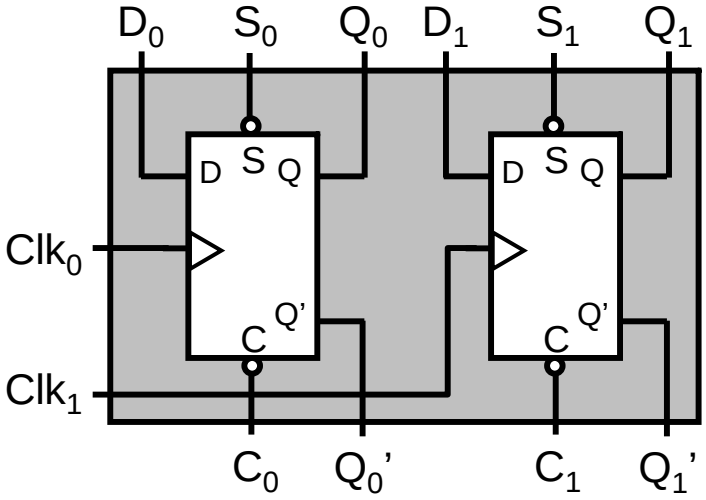


Course Roadmap

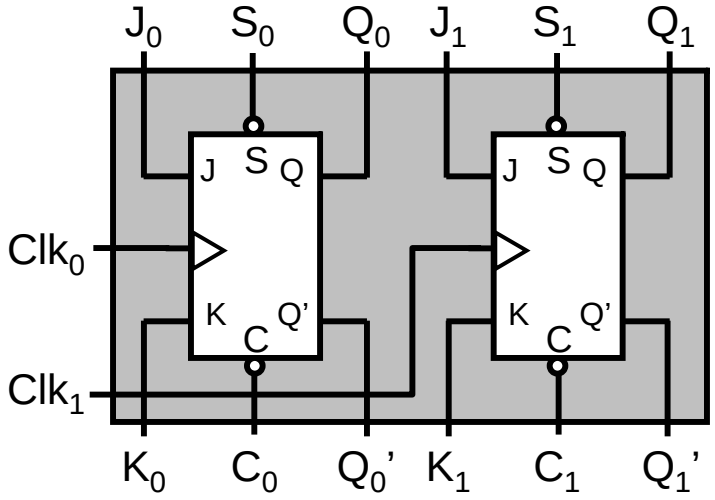


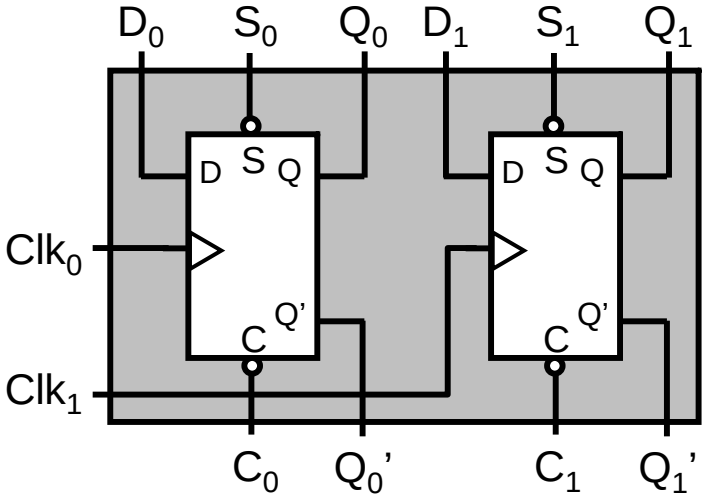
Flip-flops vs. Generic Registers

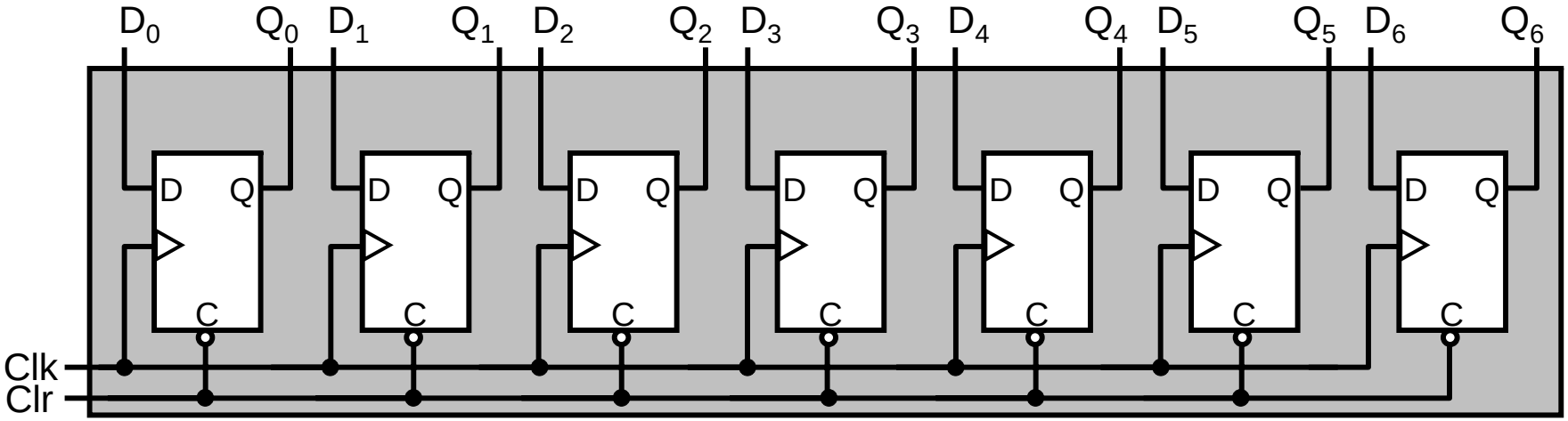




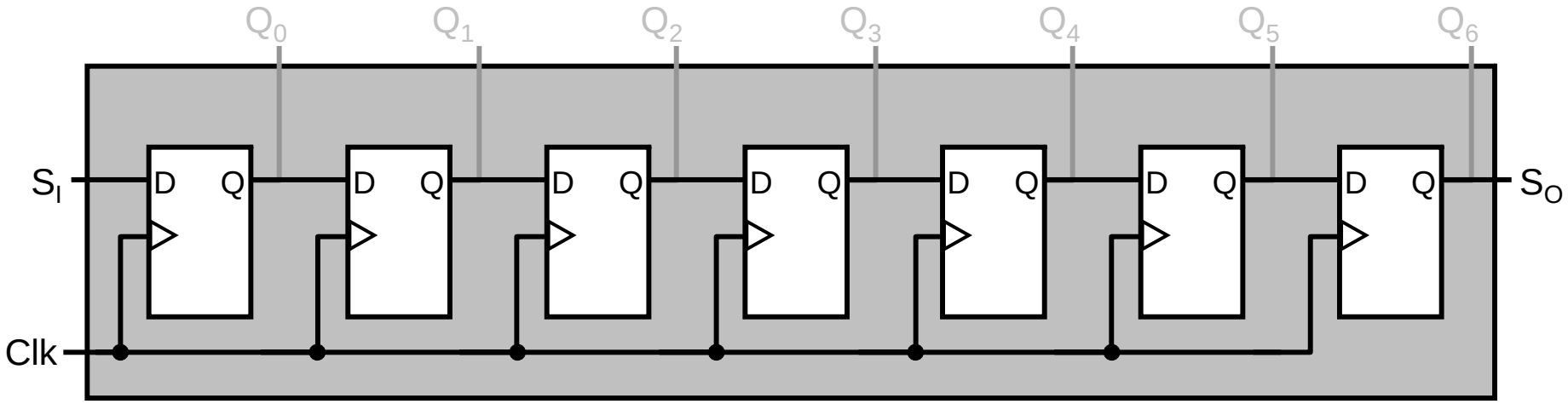
Flip-flops vs. Generic Registers



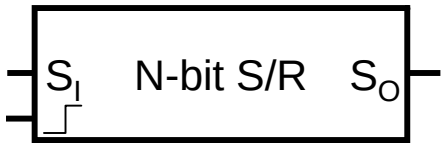




Shift Register

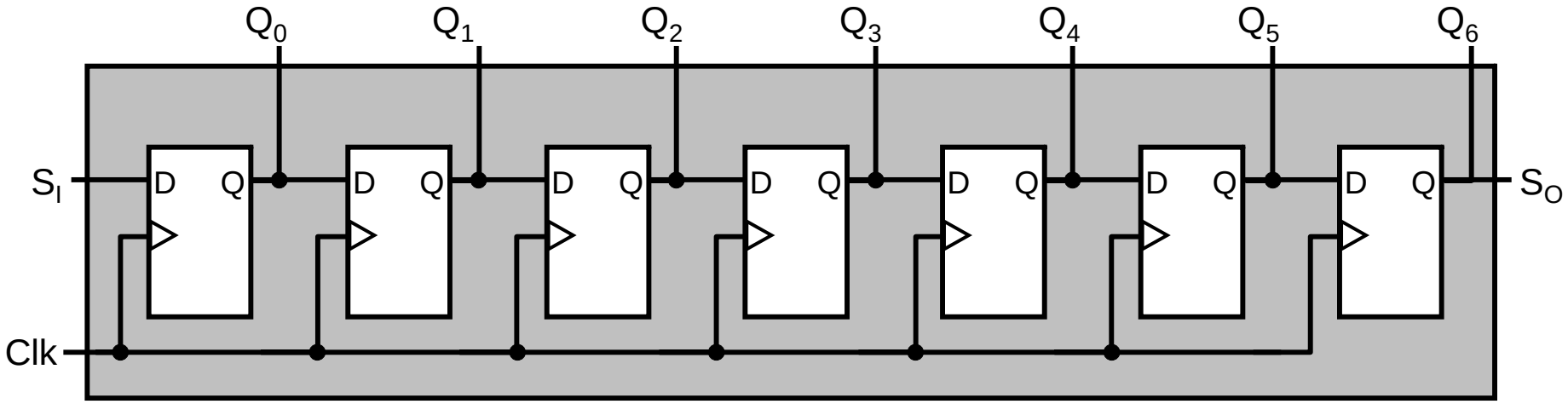


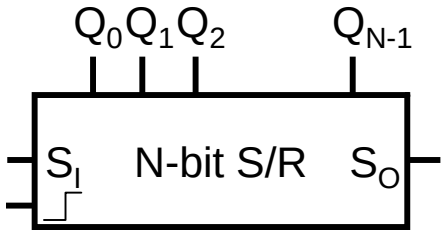
Present State	Input	Next State	Output
$Q_0\,Q_1\,Q_2\,Q_3\,Q_4\,Q_5\,Q_6$	S_I	$S_I Q_0 Q_1\,Q_2\,Q_3\,Q_4\,Q_5$	$S_0=Q_6$



SISO Register
Serial-in, Serial-out

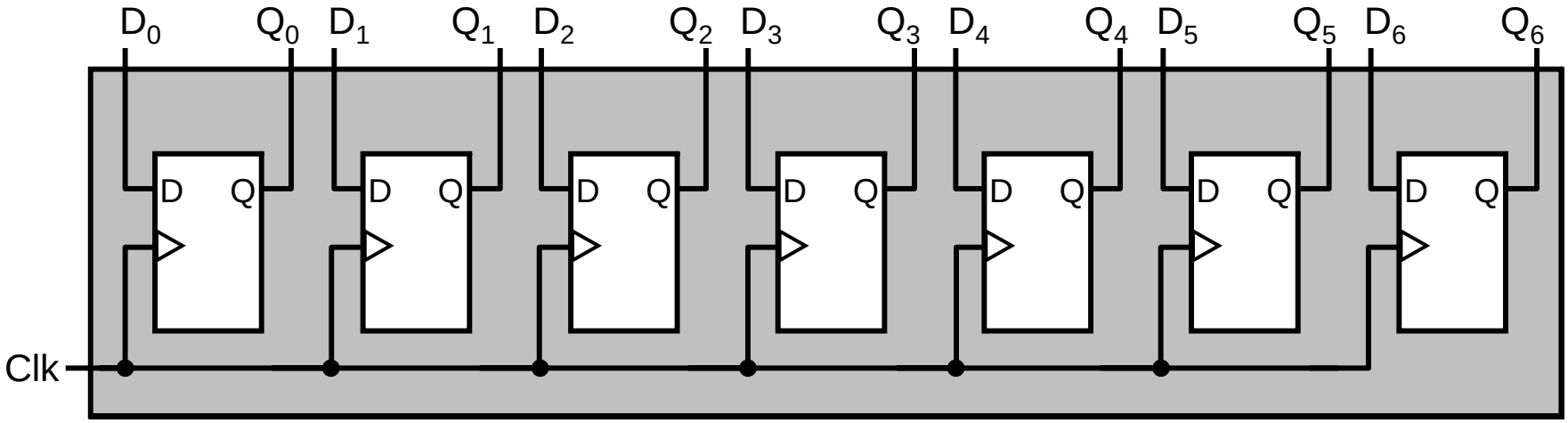
Shift Register Variants

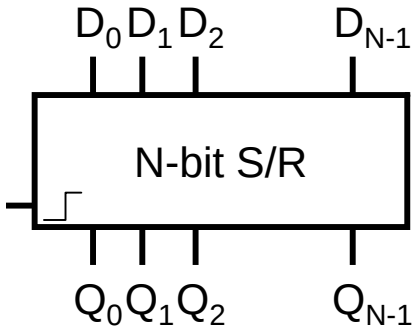




SIPO Register
Serial-in, Parallel-out

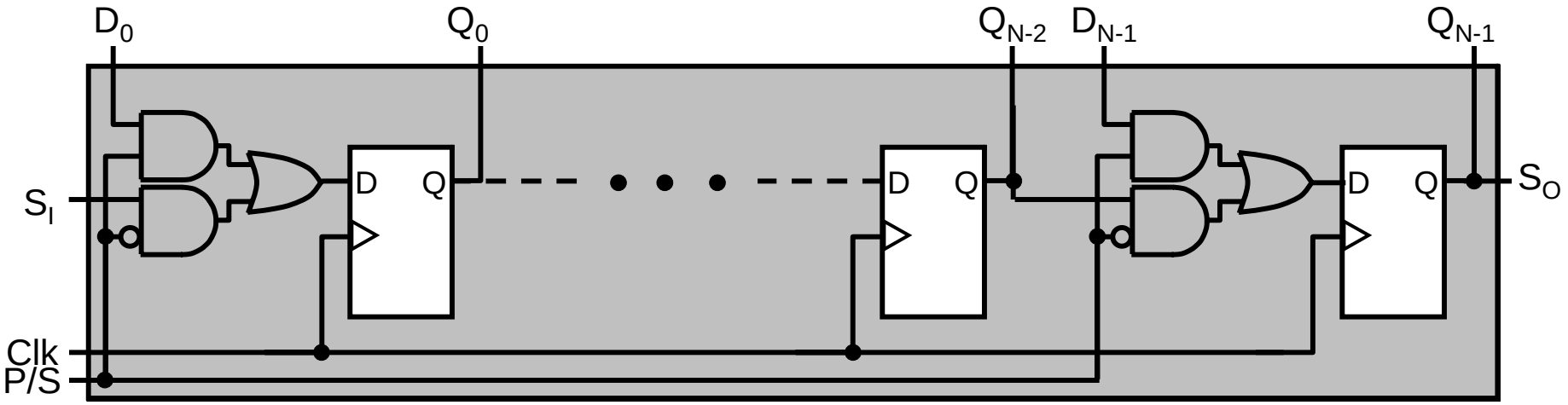
Shift Register Variants

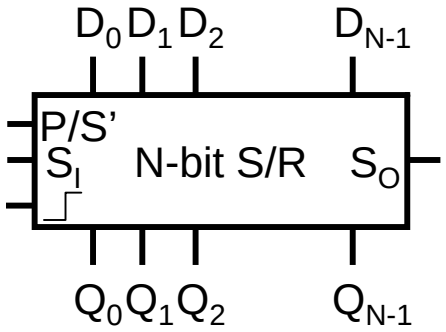




PIPO Register
Parallel-in, Parallel-out

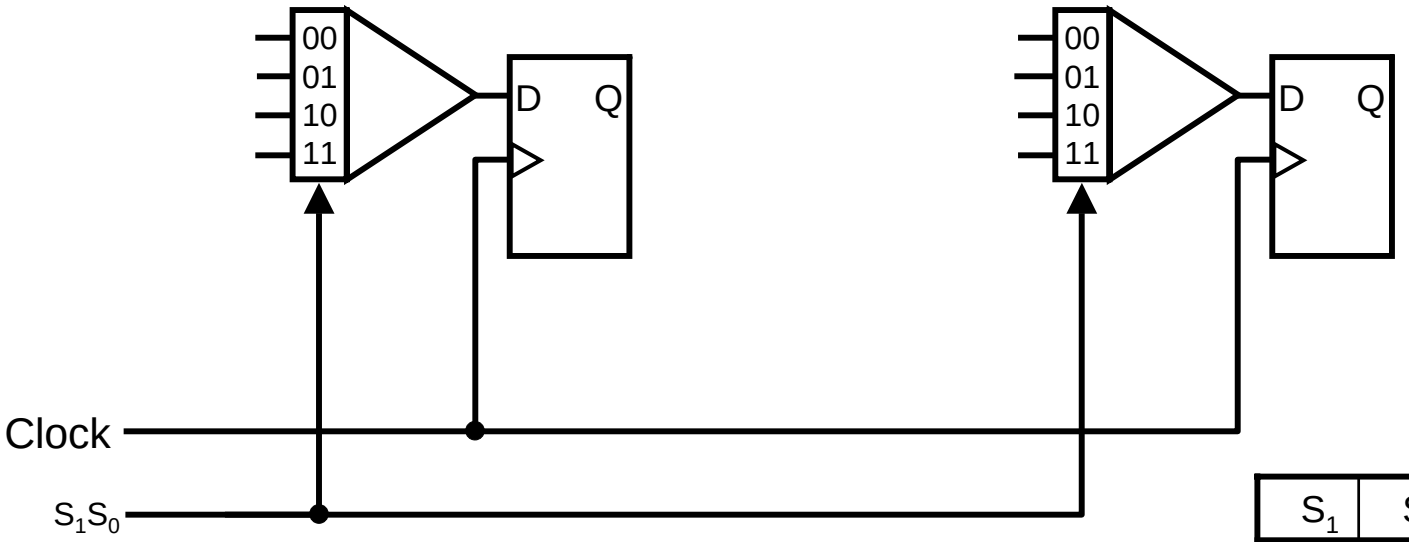
Shift Register Variants





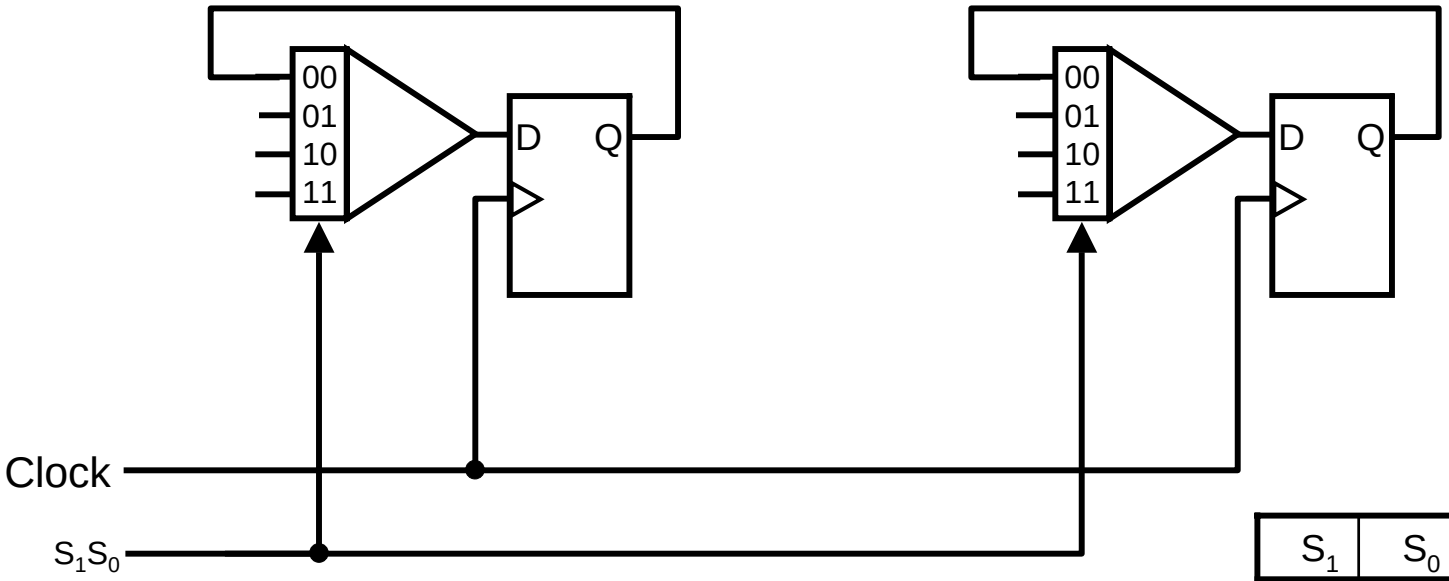
Serial/Parallel Register
Parallel-in/Serial-in,
Parallel-out/Serial-out

Shift Register Variants



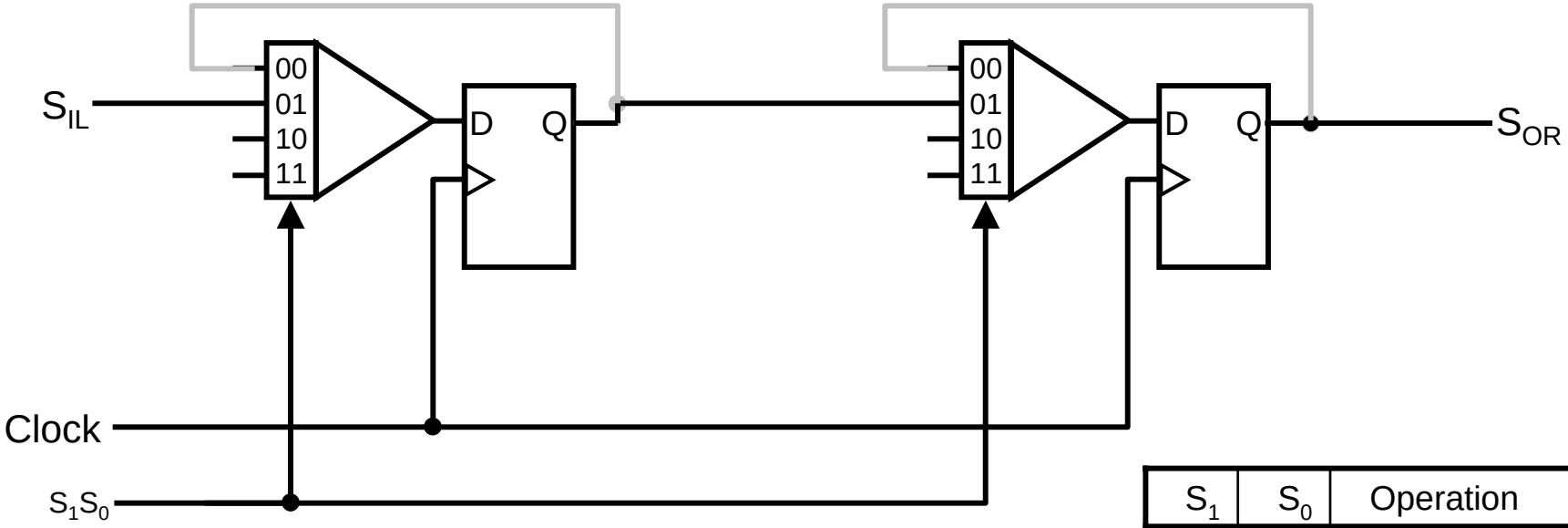
S_1	S_0	Operation

Shift Register Variants



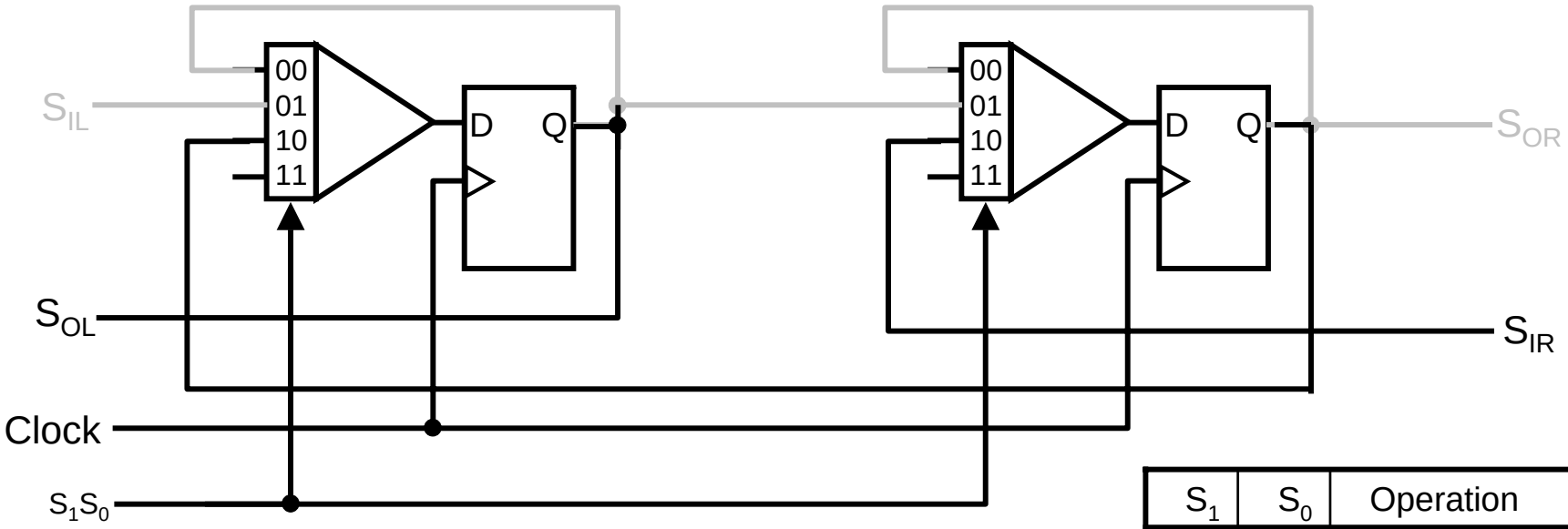
S_1	S_0	Operation
0	0	No Change

Shift Register Variants



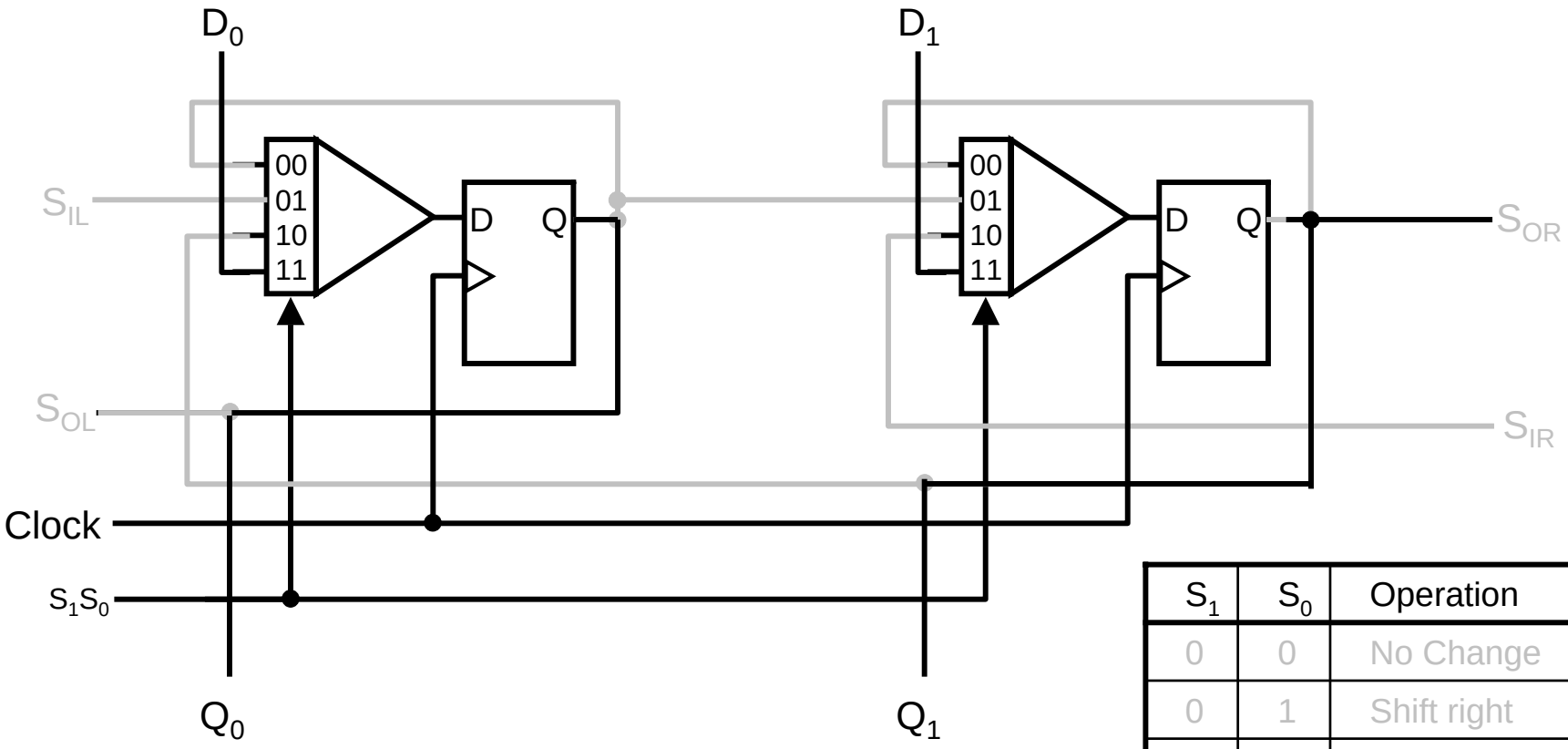
S_1	S_0	Operation
0	0	No Change
0	1	Shift right

Shift Register Variants



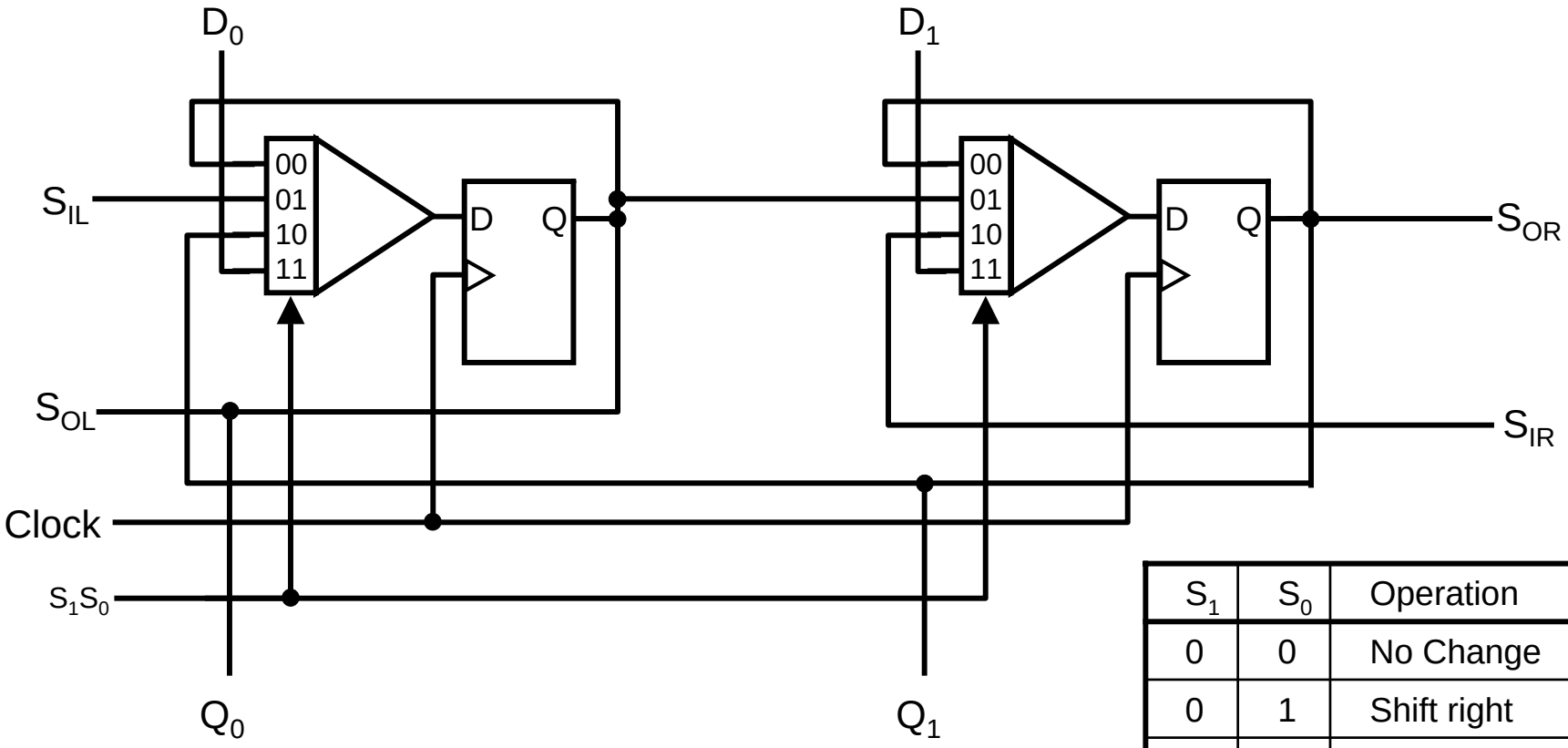
S_1	S_0	Operation
0	0	No Change
0	1	Shift right
1	0	Shift left

Shift Register Variants



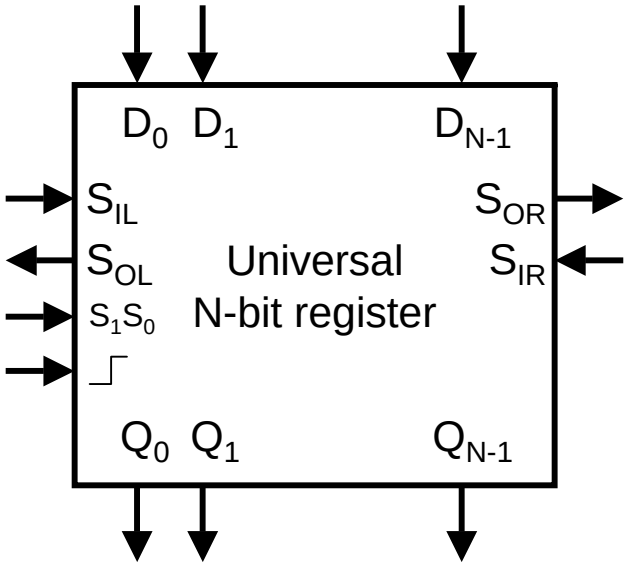
S_1	S_0	Operation
0	0	No Change
0	1	Shift right
1	0	Shift left
1	1	Parallel load

Shift Register Variants



S_1	S_0	Operation
0	0	No Change
0	1	Shift right
1	0	Shift left
1	1	Parallel load

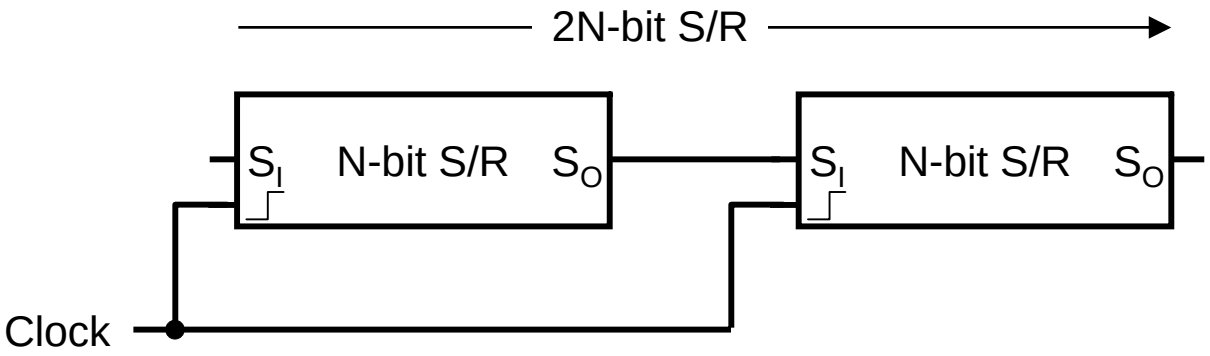
Shift Register Variants



S_1	S_0	Operation
0	0	No Change
0	1	Shift right
1	0	Shift left
1	1	Parallel load

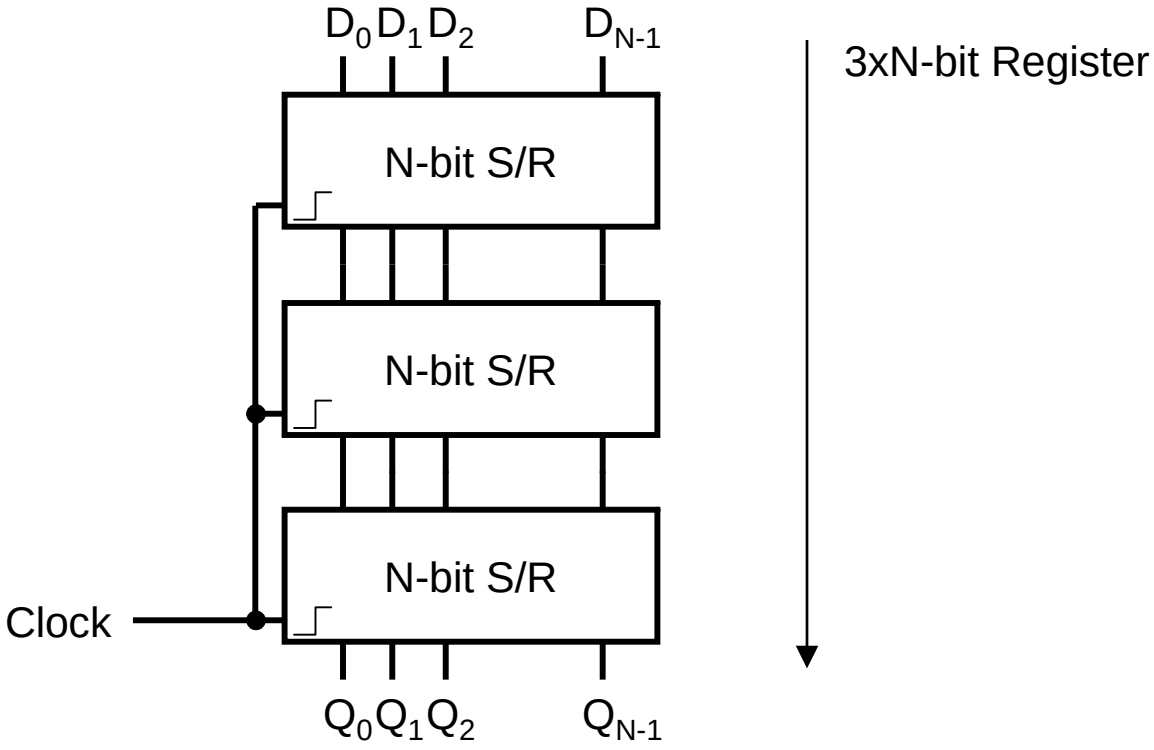
Tandem S/Rs

- Serial registers



Tandem S/Rs

- Parallel registers



Summary

- Fundamental concepts of digital systems (Mano Chapter 1)
- Binary codes, number systems, and arithmetic (Ch 1)
- Boolean algebra (Ch 2)
- Simplification of switching equations (Ch 3)
- Digital device characteristics (e.g., TTL, CMOS)/design considerations (Ch 10)
- Combinatoric logical design including LSI implementation (Chapter 4)
- Flip-flops and state memory elements (Ch 5)
- Sequential logic analysis and design (Ch 5)
- Counters, shift register circuits (Ch 6)
- Hazards, Races, and time related issues in digital design (Ch 9)
- Synchronous vs. asynchronous design (Ch 9)
- Memory and Programmable logic (Ch 7)
- Minimization of sequential systems
- Introduction to Finite Automata

Homework 9 – due in Class 11

- As always, show all work
- Problems 5-16, 5-17, 5-18, 5-19, 6-4
- Design a 3-bit Universal Shift Register using AND, OR, NOT, NAND or NOR gates and D Flip-flops that implements the following functions

S_1	S_0	Function
0	0	Shift left
0	1	Shift right
1	0	Parallel load from top
1	1	Parallel load from bottom

  - The shift register has top and bottom D inputs and Q outputs, as well as right and left shift-in inputs and shift-out outputs