

**CpE358/CS381**

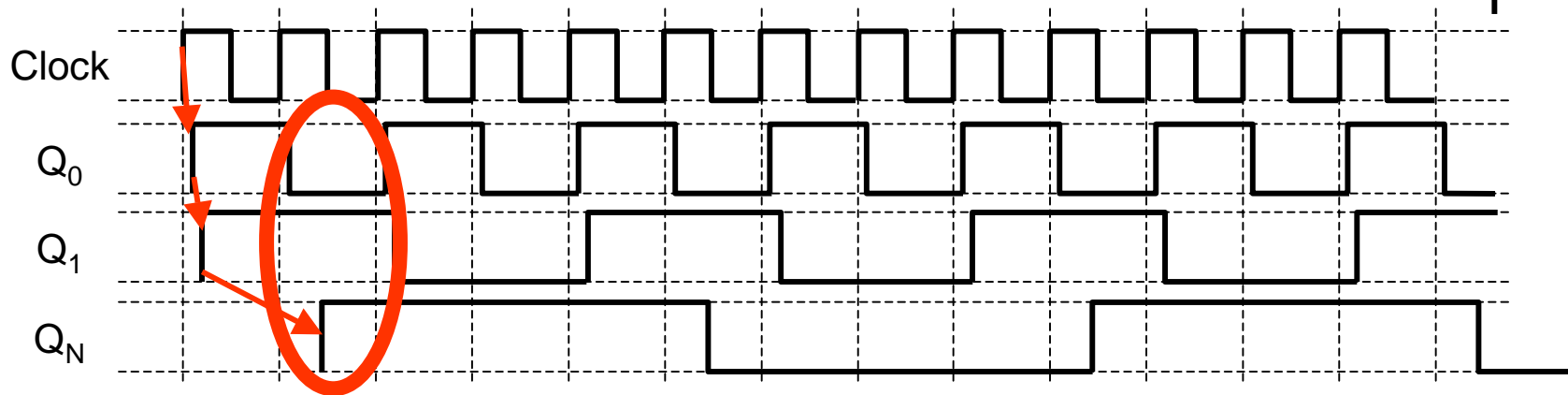
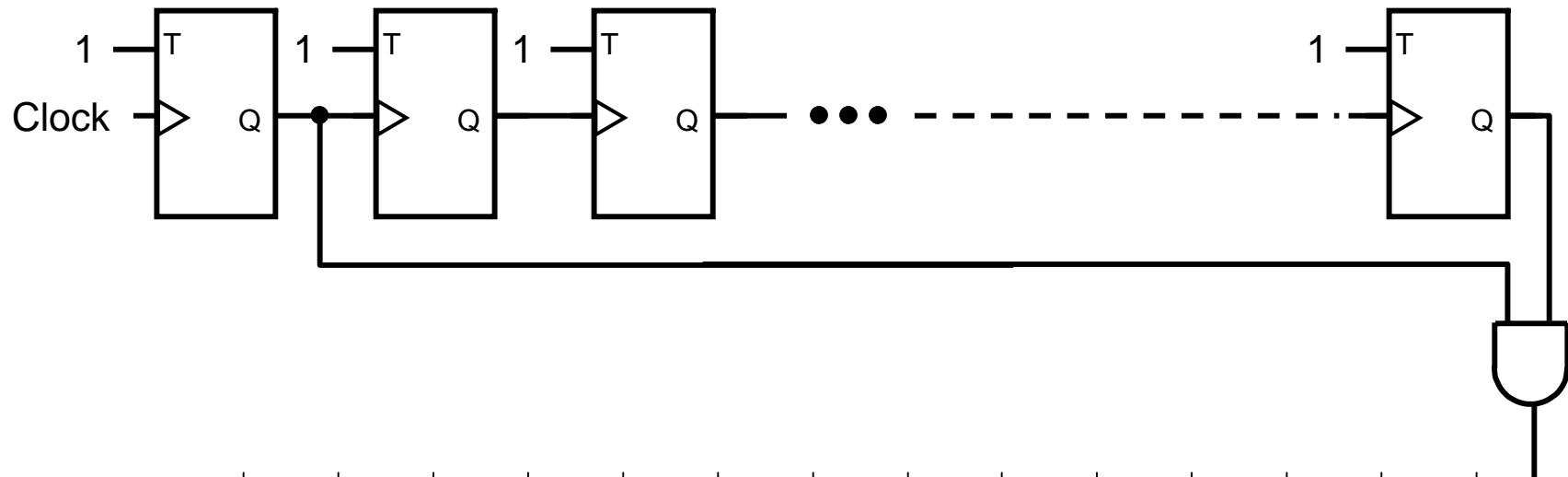
**Switching Theory and  
Logical Design**

**Class 11**

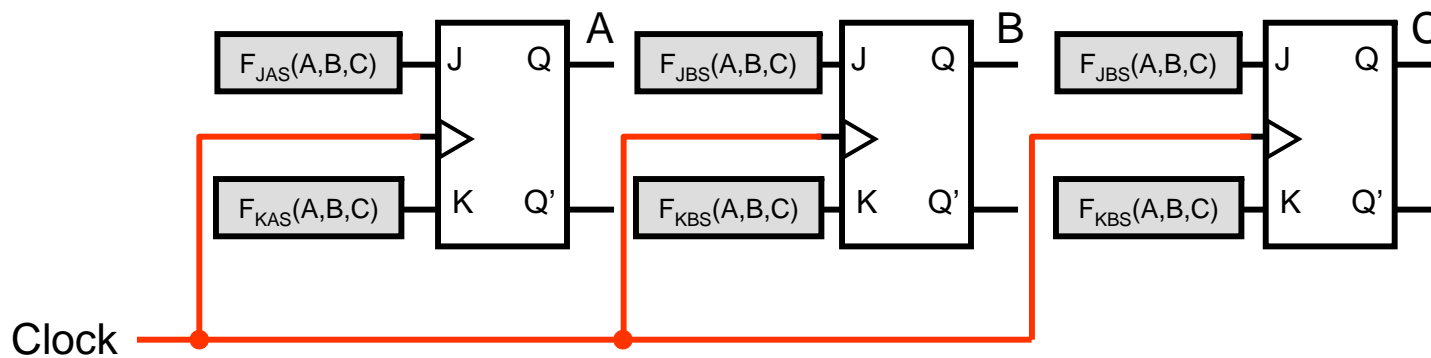
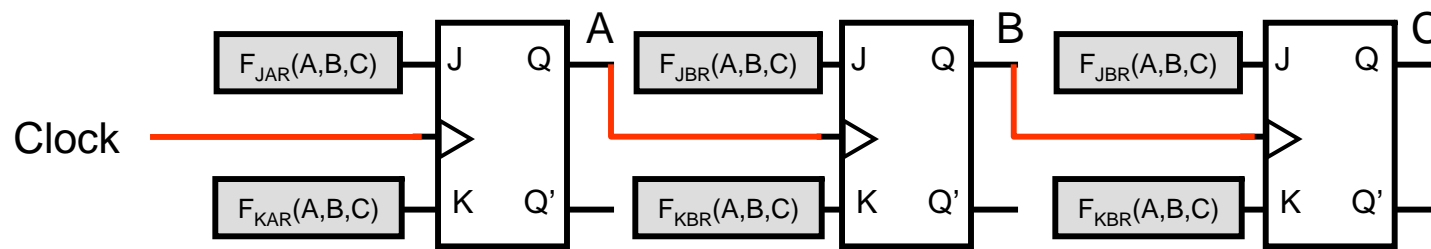
# Today

- Fundamental concepts of digital systems (Mano Chapter 1)
- Binary codes, number systems, and arithmetic (Ch 1)
- Boolean algebra (Ch 2)
- Simplification of switching equations (Ch 3)
- Digital device characteristics (e.g., TTL, CMOS)/design considerations (Ch 10)
- Combinatoric logical design including LSI implementation (Chapter 4)
- Flip-flops and state memory elements (Ch 5)
- Sequential logic analysis and design (Ch 5)
- Counters, shift register circuits (Ch 6)
- Hazards, Races, and time related issues in digital design (Ch 9)
- Synchronous vs. asynchronous design (Ch 9)
- Memory and Programmable logic (Ch 7)
- Minimization of sequential systems
- Introduction to Finite Automata

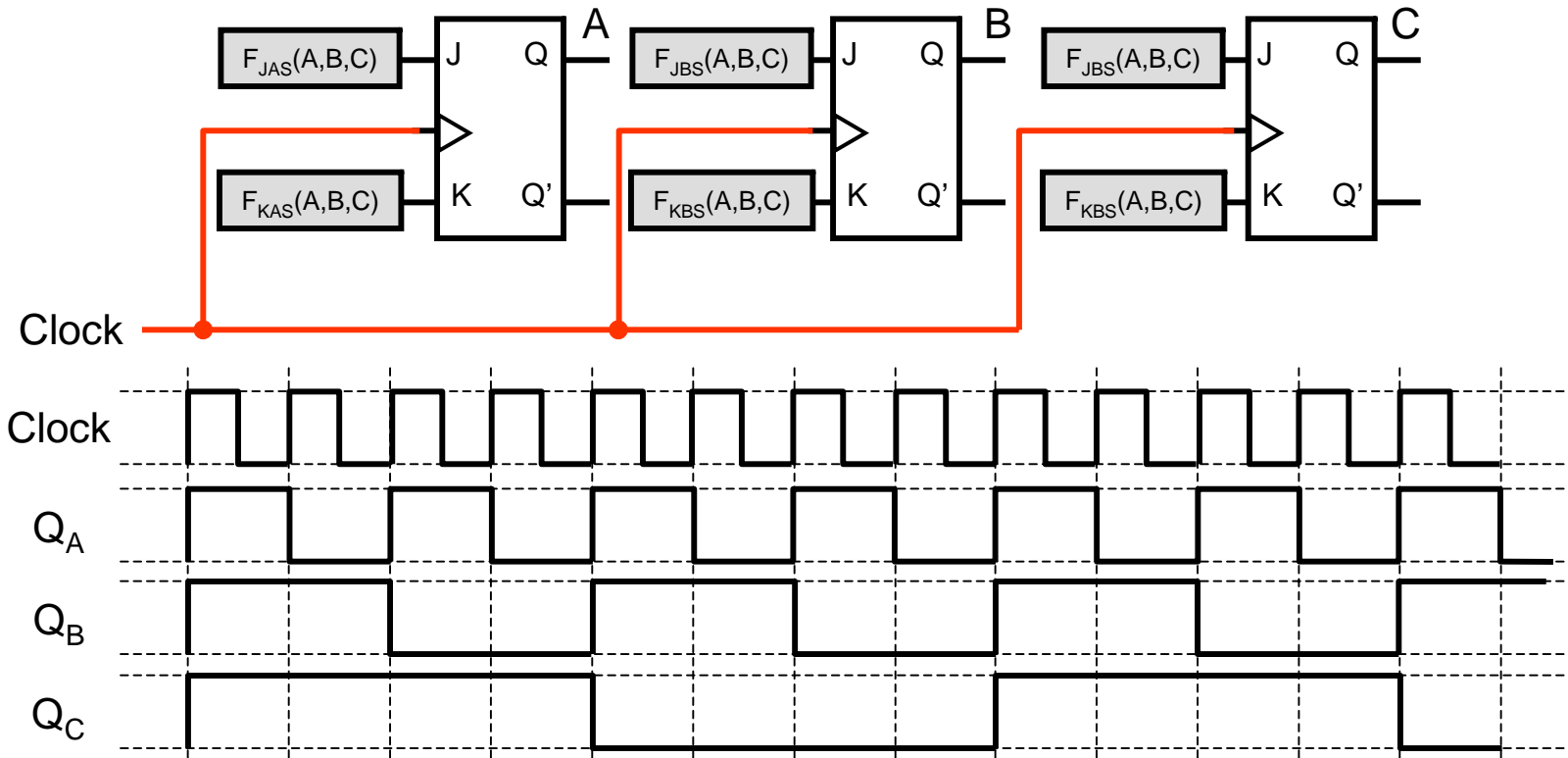
# Cascading Counters



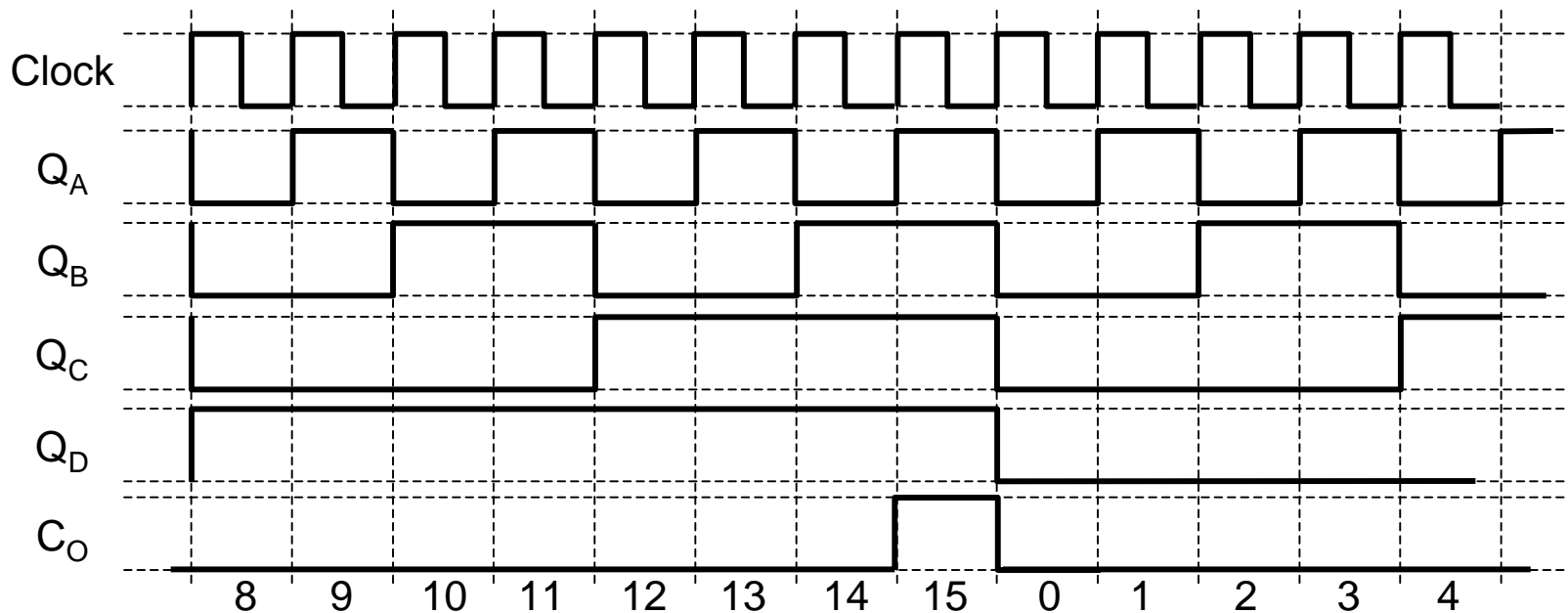
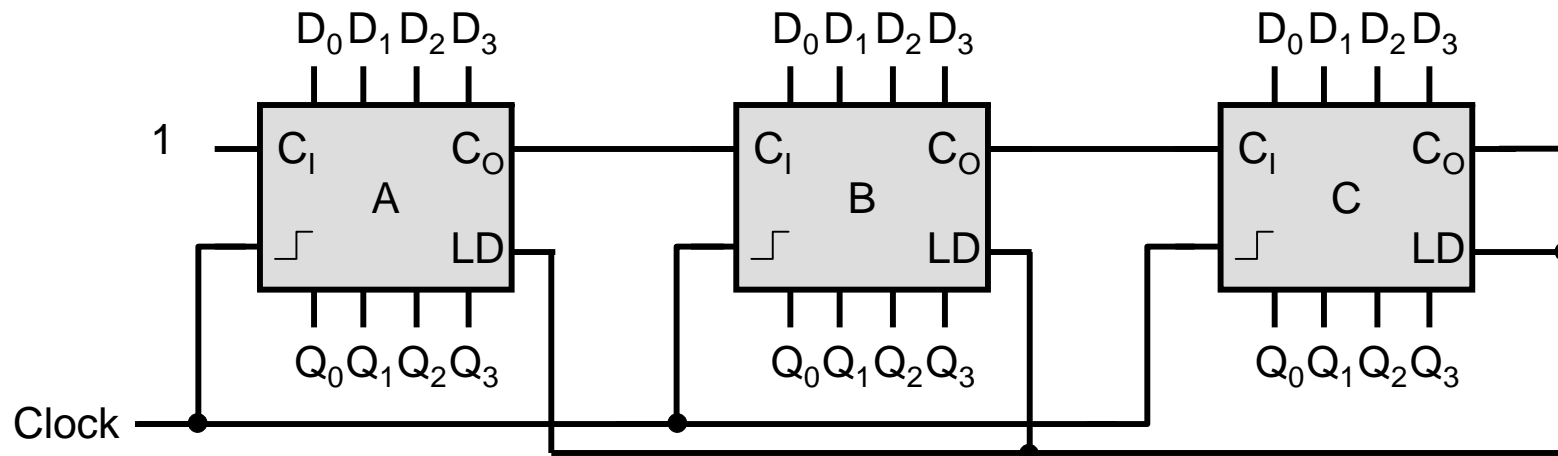
# Ripple Counters vs. Synchronous Counters



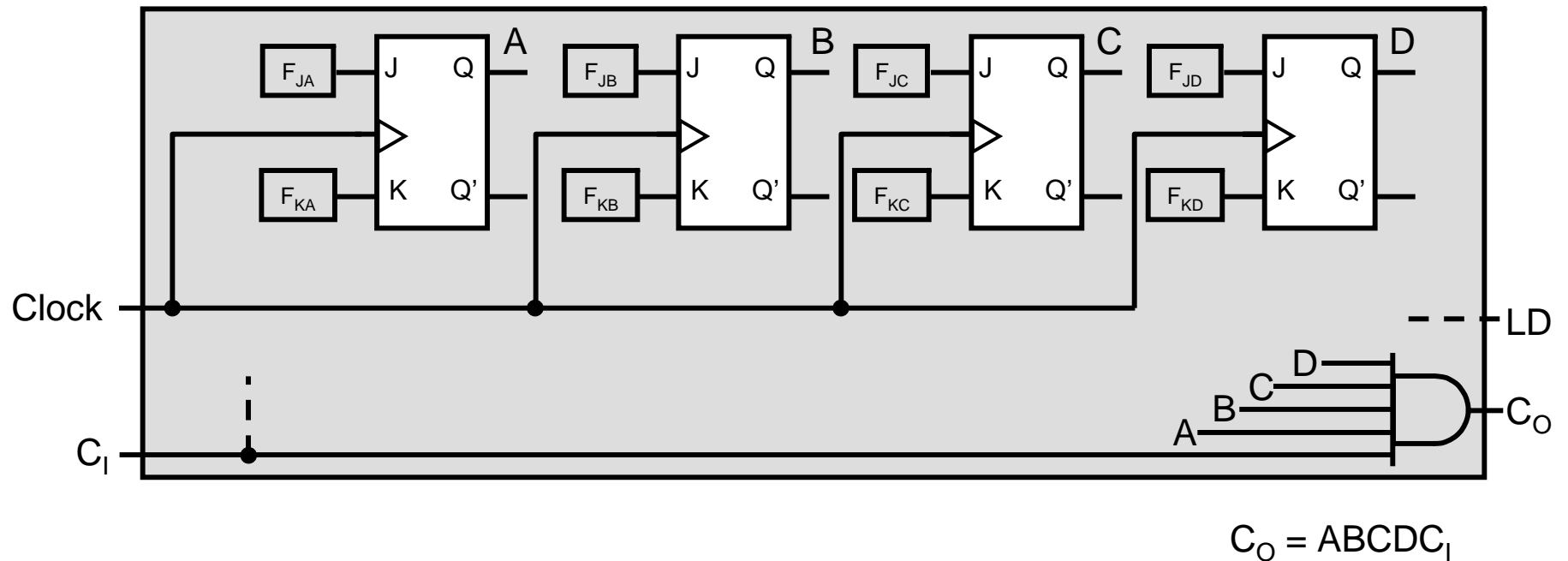
# Synchronous Counters



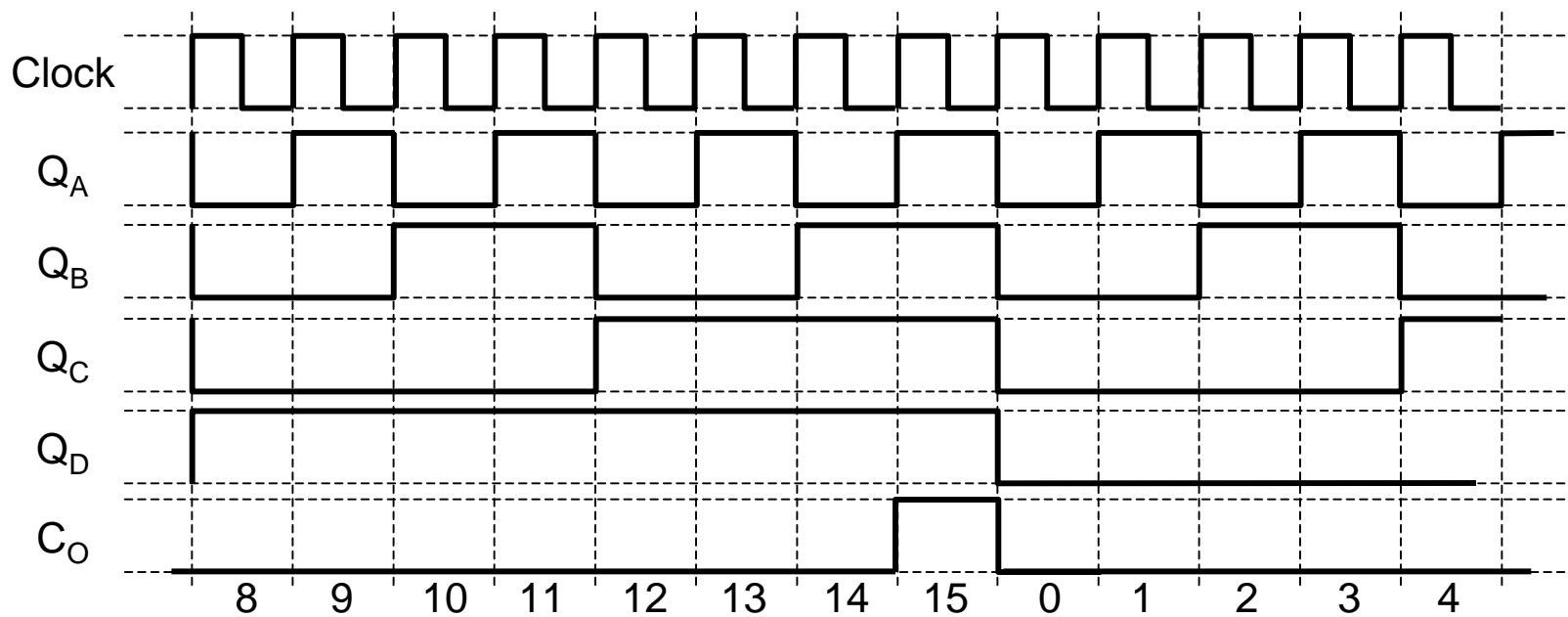
# Cascaded Synchronous Counters



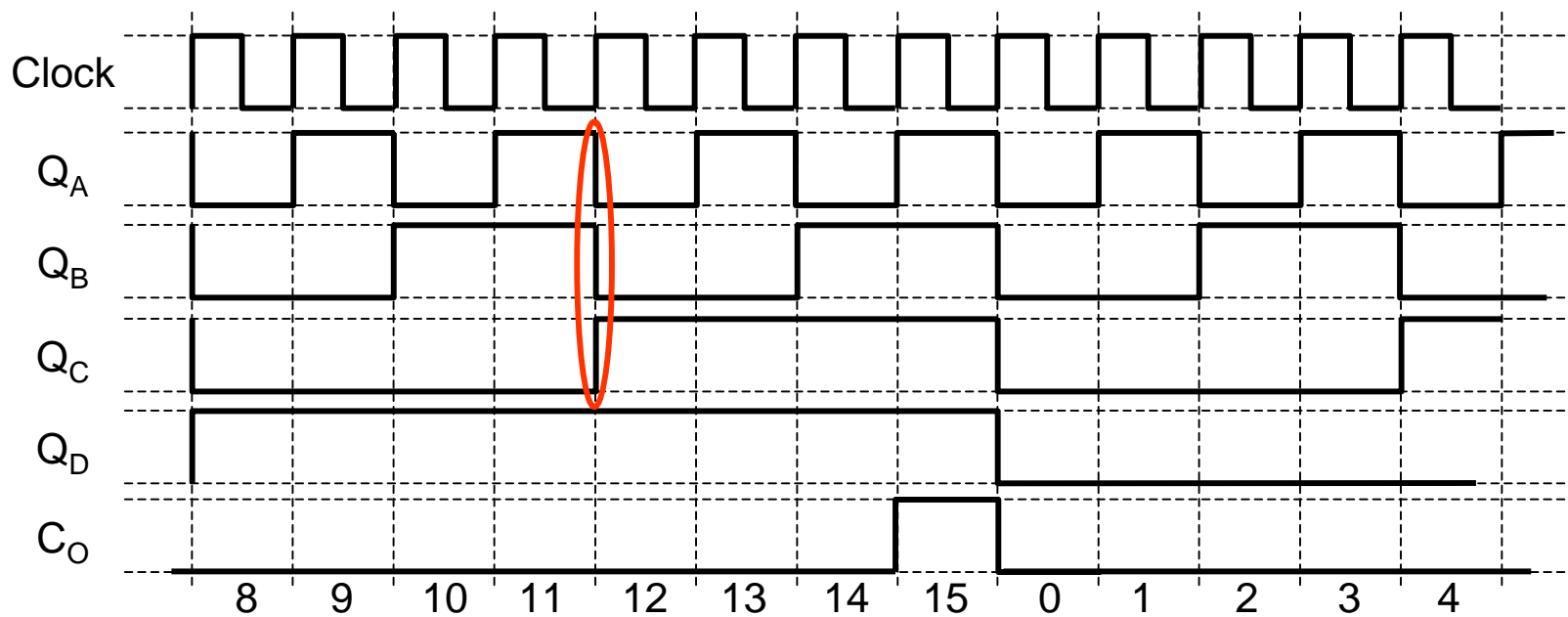
# 74163 Synchronous 4-bit counter



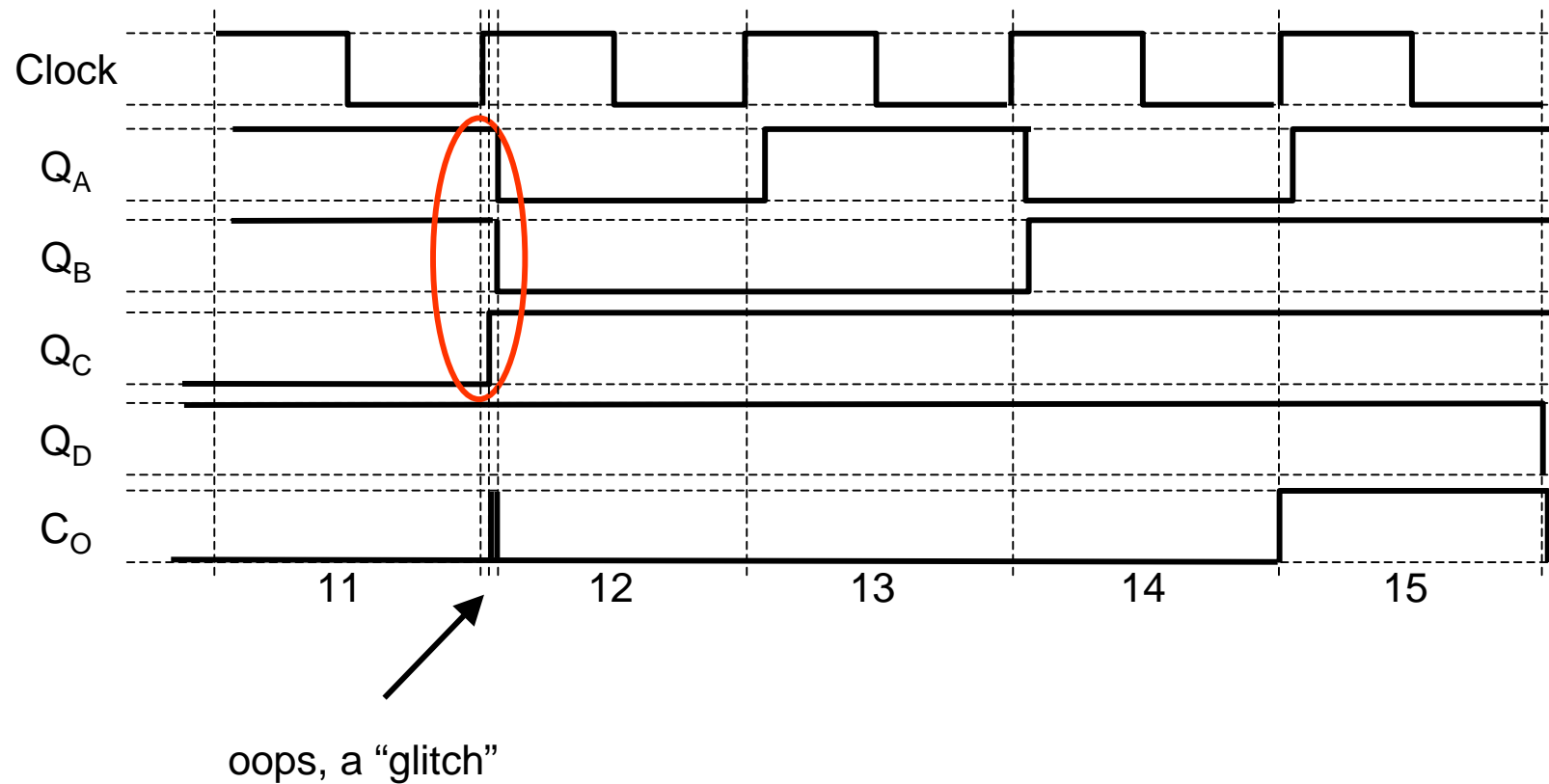
# 74163 Synchronous 4-bit counter



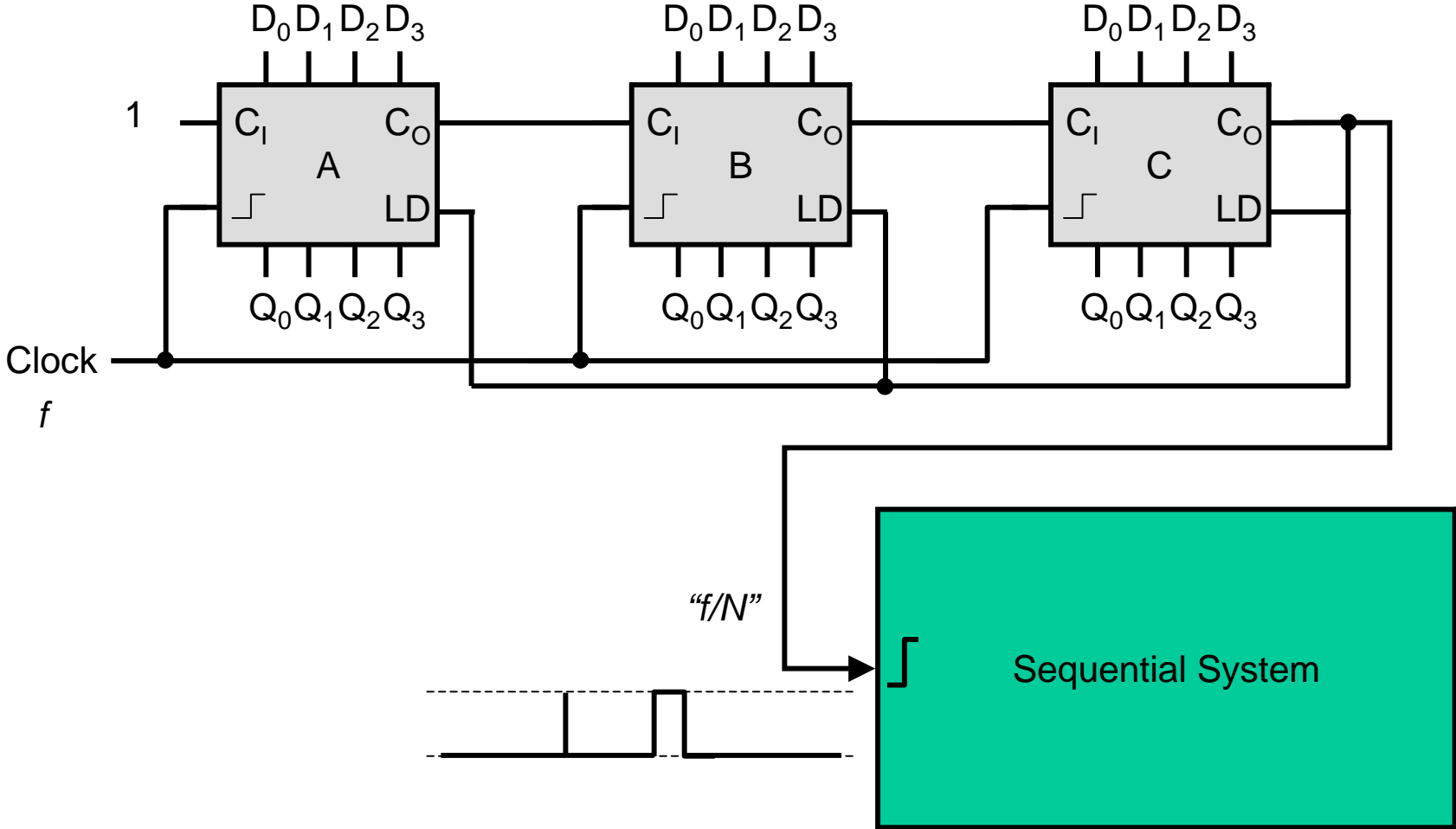
# 74163 Synchronous 4-bit counter



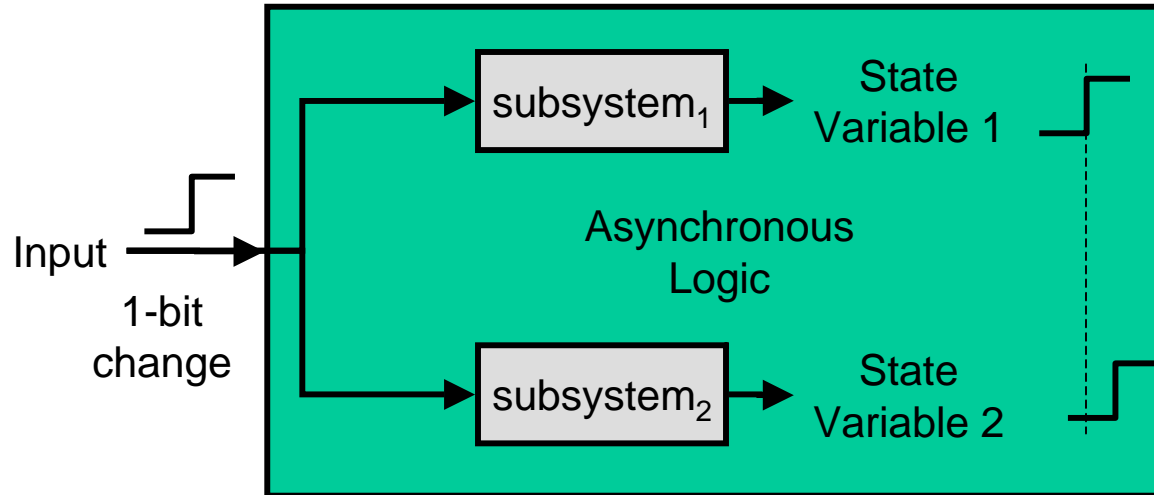
# 74163 Synchronous 4-bit counter



# Implications of "Glitch"



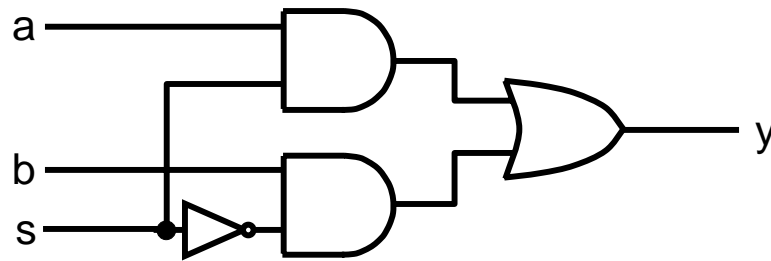
# “Race” Conditions



- Which occurs first?
- What effect does the order of change have on system operation?

# “Hazards”

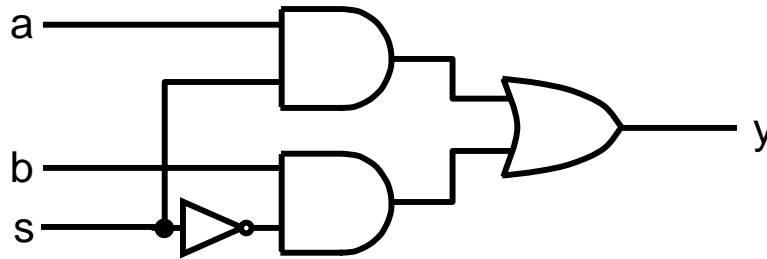
- s selects either a or b:



$$y = sa + s'b$$

# “Hazards”

- s selects either a or b:

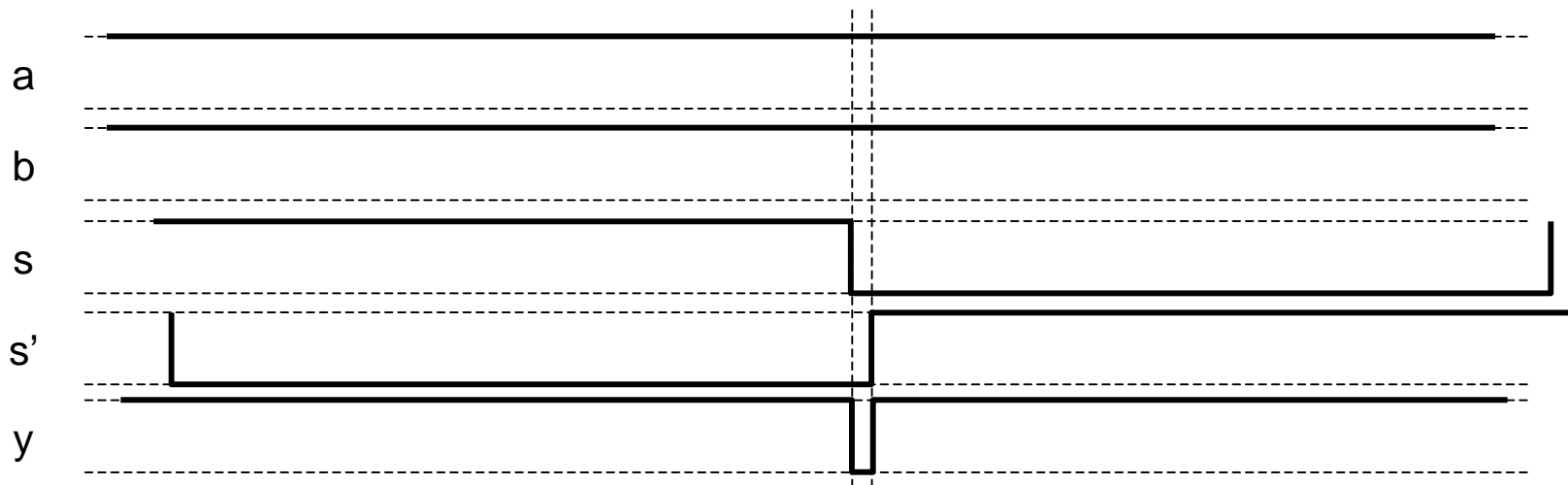
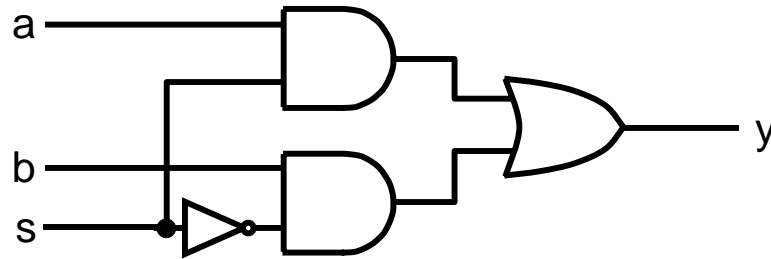


$$y = sa + s'b$$

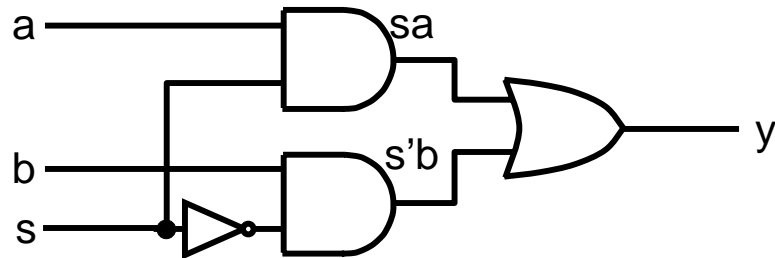
- What if a and b are both 1?

$$y = s1 + s'1 = s + s' = 1$$

# “Hazards”



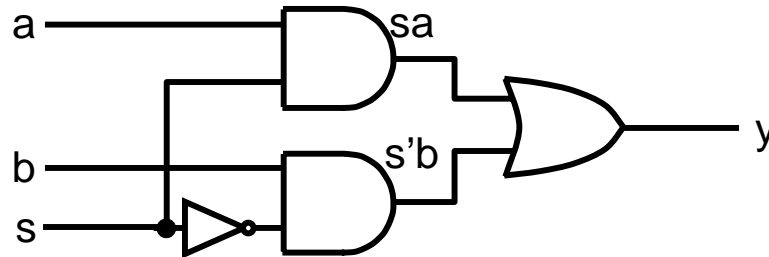
# “Hazards”



$s \backslash ab$	00	01	11	10
0	0	1	1	0
1	0	0	1	1

Arrows indicate the following:  $s'b$  points to the 11 column header, and  $sa$  points to the 11 row header. Red boxes highlight the 1s in the 01 and 11 cells of the 0 row, and the 1s in the 11 and 10 cells of the 1 row.

# “Hazards”



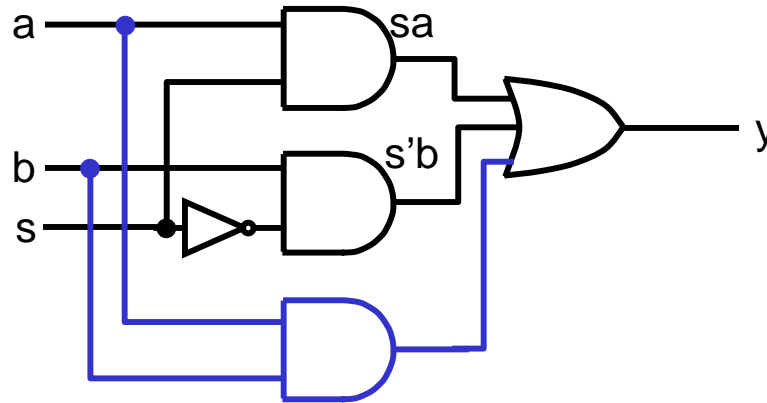
s \ ab	00	01	11	10
0	0	1	1	0
1	0	0	1	1

An arrow labeled  $s'b$  points to the top row of the table (s=0).  
 An arrow labeled  $sa$  points to the rightmost column of the table (a=1).  
 Red boxes highlight the cells (0,1), (0,11), (1,1), and (1,11).  
 A red arrow points from the cell (0,11) down to the cell (1,11).

Transition in  $s$  is causing system to move between two **separate** covers.

The region between covers is undefined

# “Hazards”



s \ ab	00	01	11	10
0	0	1	1	0
1	0	0	1	1

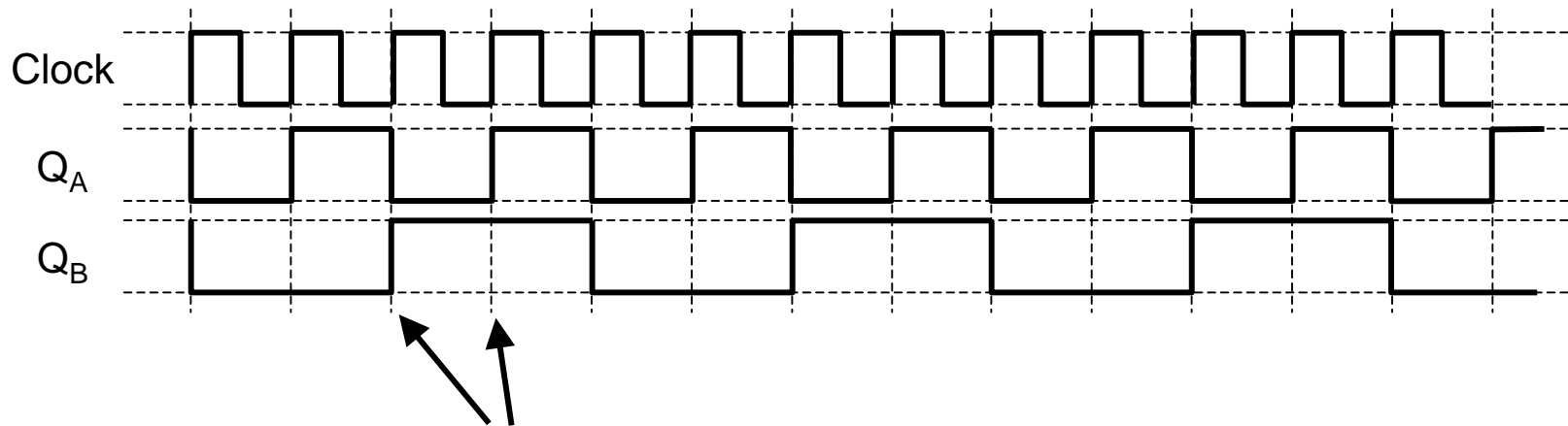
Transition in  $s$  is causing system to move between two **separate** covers.

The region between covers is undefined

**Solution:** eliminate uncovered region

# Why Asynchronous Logic?

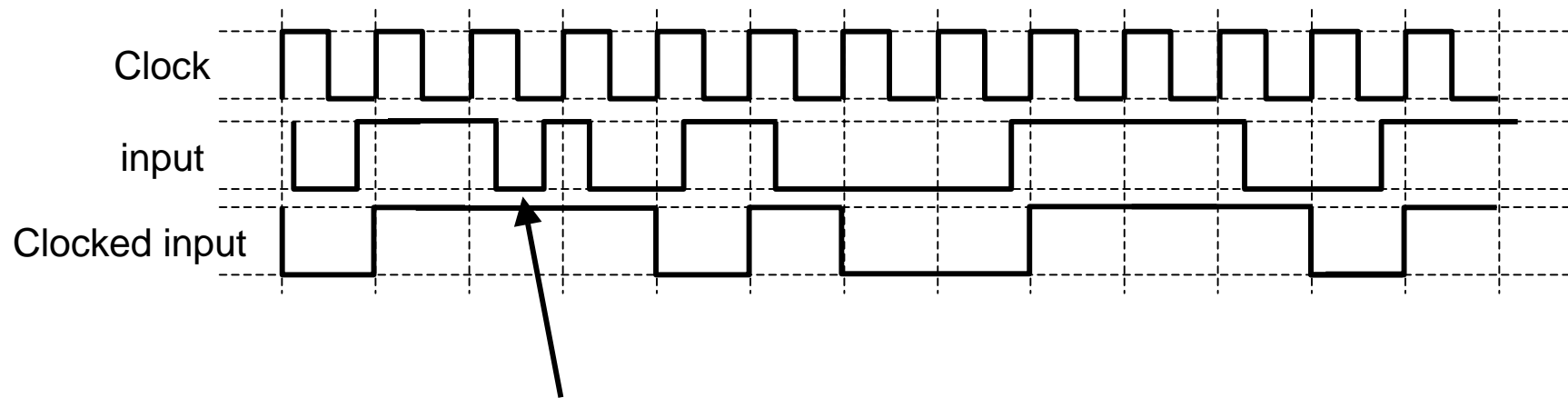
## 1. Speed



Nothing happens at rates faster than fastest clock

# Why Asynchronous Logic?

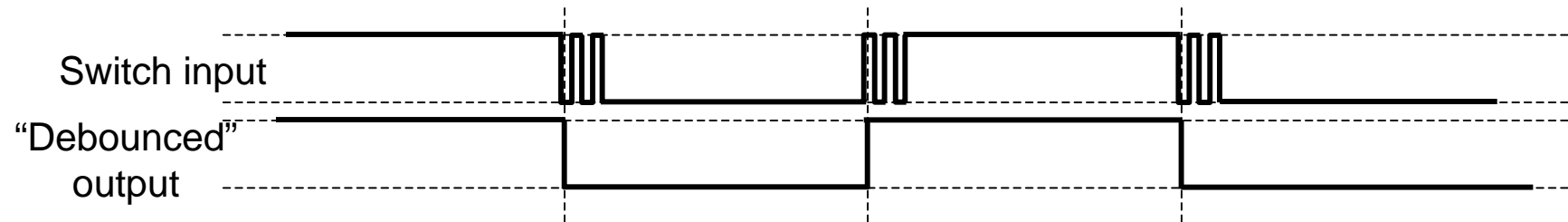
## 2. The Asynchronous Universe



Events that occur between clock cycles are missed

# Why Asynchronous Logic?

3. Some things are easier with asynchronous logic



# Summary

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# Homework 11 – due in Class 13

- No homework