

CpE358/CS381

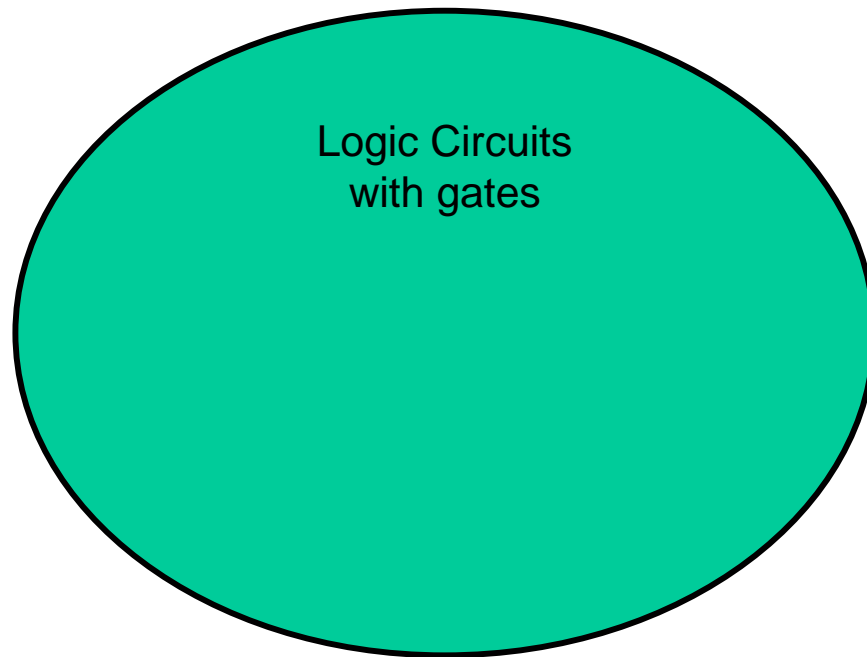
**Switching Theory and
Logical Design**

Class 10

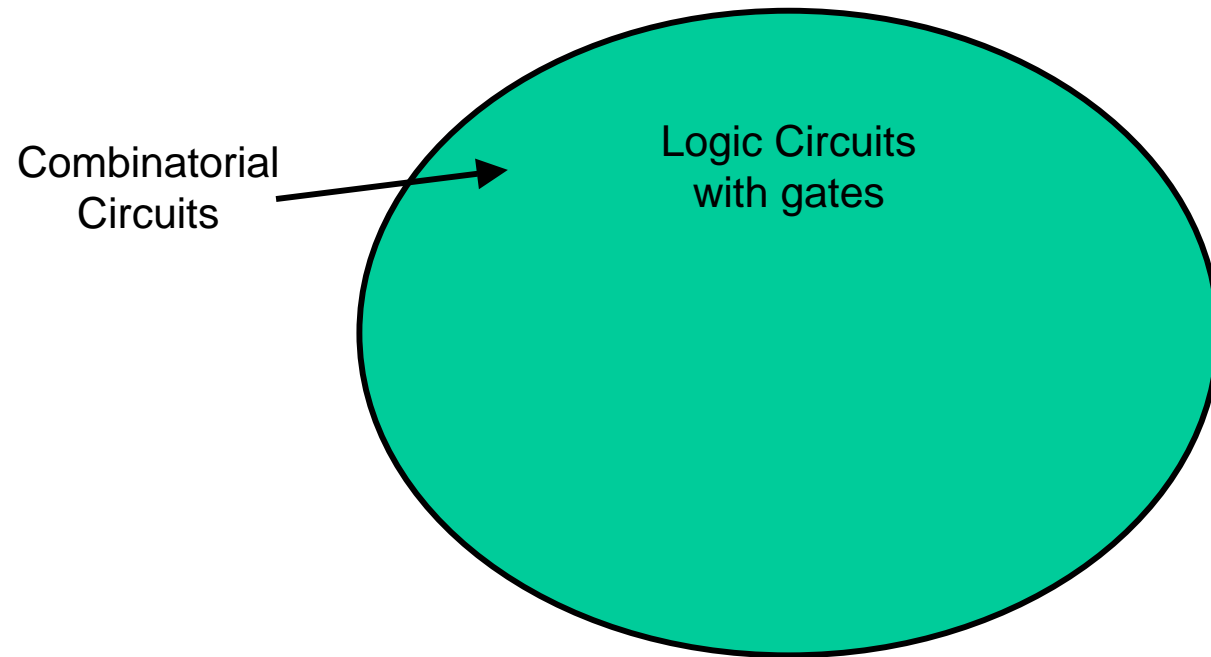
Today

- Fundamental concepts of digital systems (Mano Chapter 1)
- Binary codes, number systems, and arithmetic (Ch 1)
- Boolean algebra (Ch 2)
- Simplification of switching equations (Ch 3)
- Digital device characteristics (e.g., TTL, CMOS)/design considerations (Ch 10)
- Combinatoric logical design including LSI implementation (Chapter 4)
- Flip-flops and state memory elements (Ch 5)
- Sequential logic analysis and design (Ch 5)
- **Counters, shift register circuits (Ch 6)**
- Hazards, Races, and time related issues in digital design (Ch 9)
- Synchronous vs. asynchronous design (Ch 9)
- Memory and Programmable logic (Ch 7)
- Minimization of sequential systems
- Introduction to Finite Automata

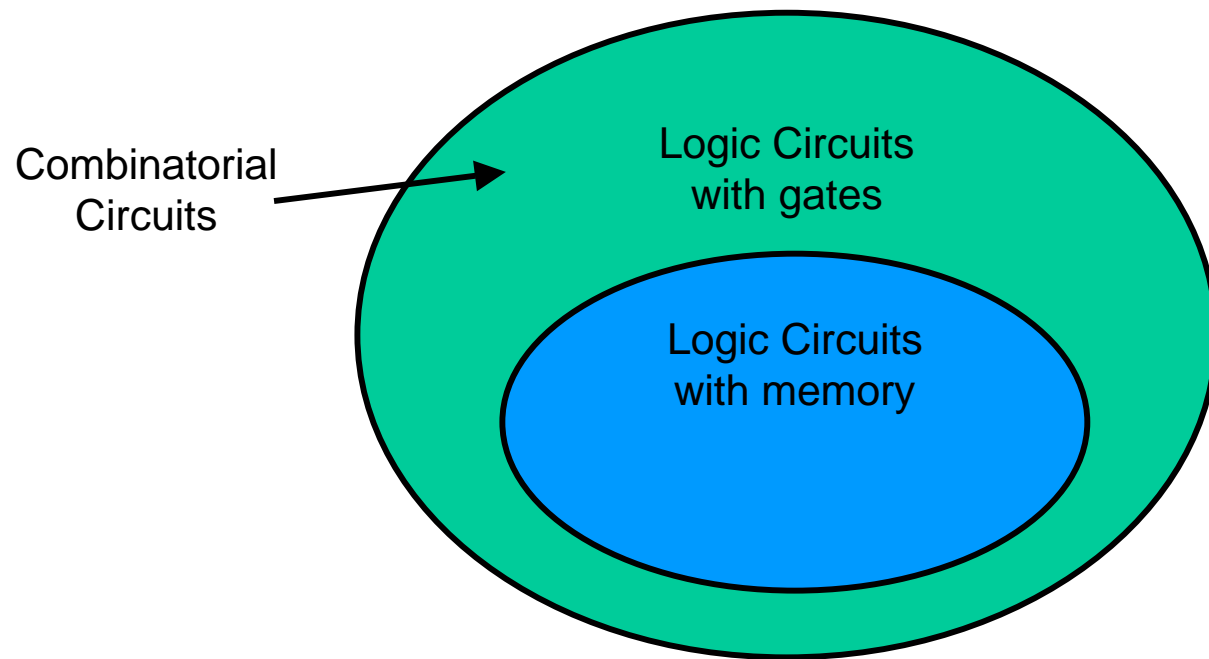
Course Roadmap



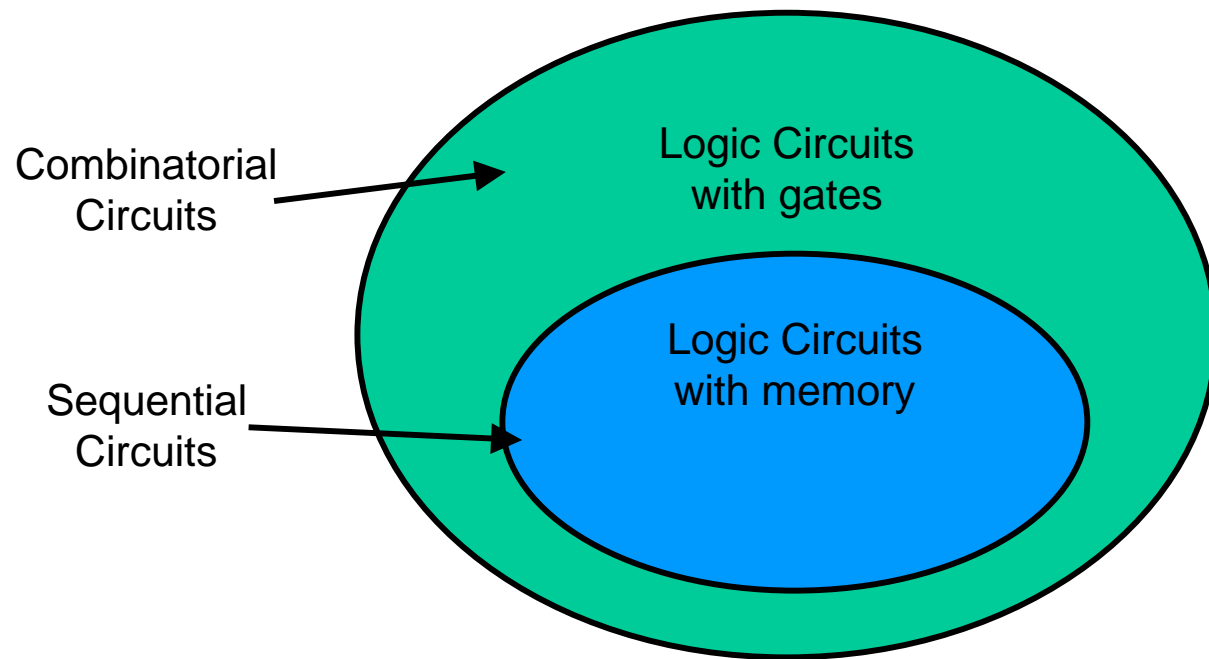
Course Roadmap



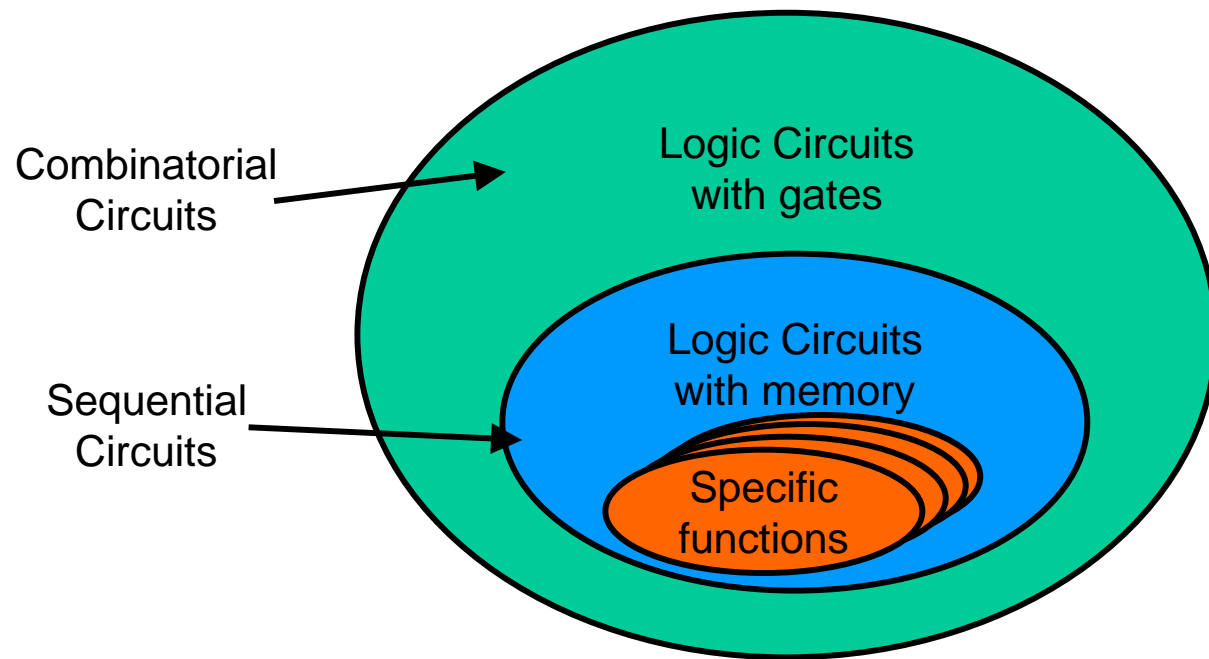
Course Roadmap



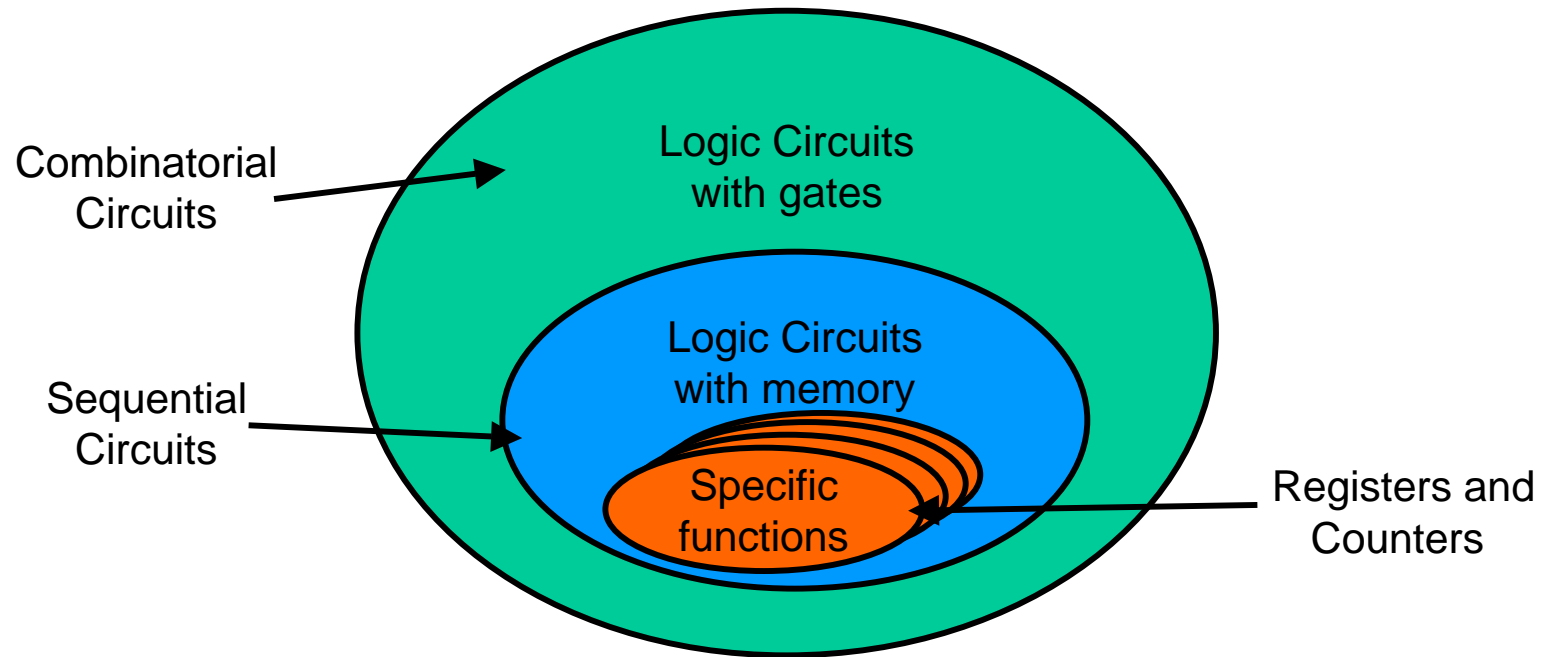
Course Roadmap



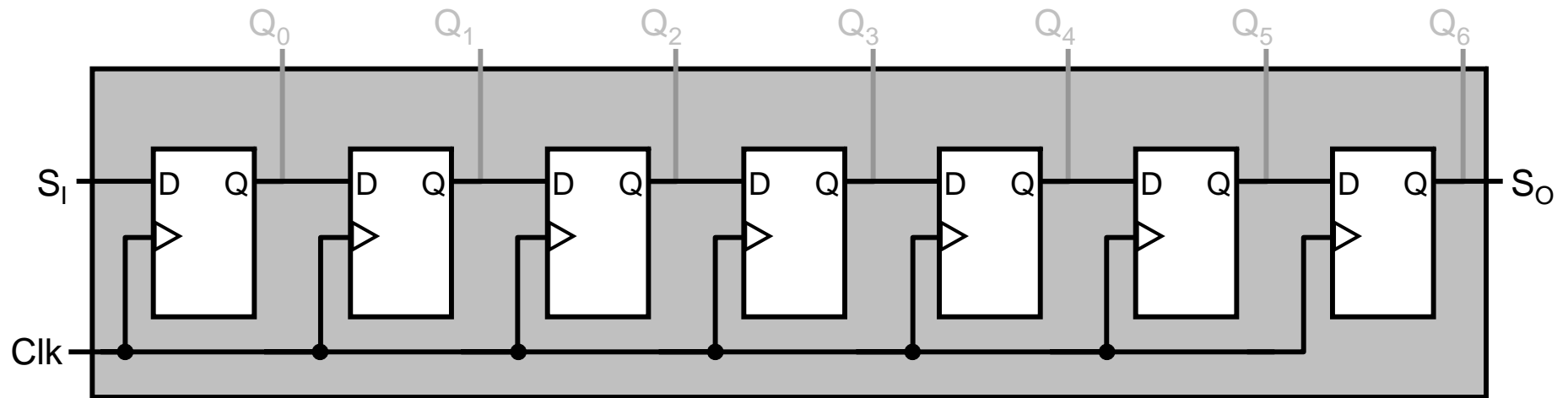
Course Roadmap



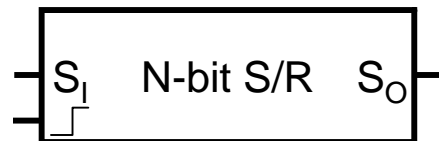
Course Roadmap



Shift Register

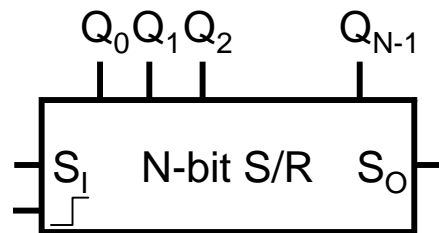
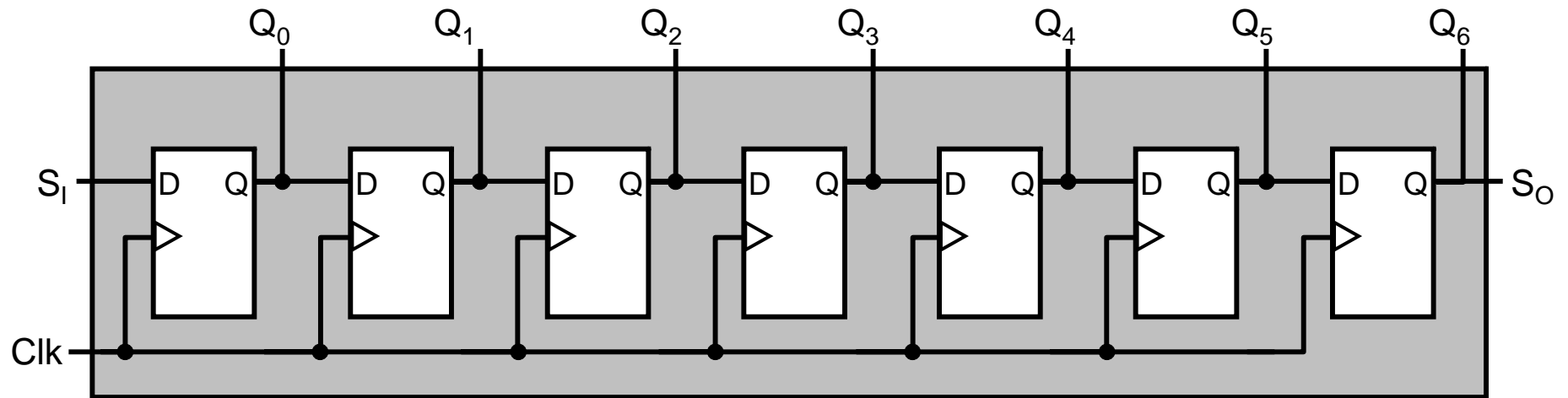


Present State	Input	Next State	Output
$Q_0 Q_1 Q_2 Q_3 Q_4 Q_5 Q_6$	S_1	$S_1 Q_0 Q_1 Q_2 Q_3 Q_4 Q_5$	$S_0 = Q_6$



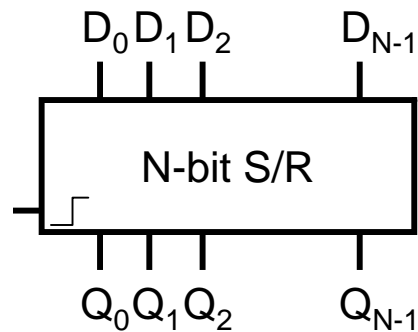
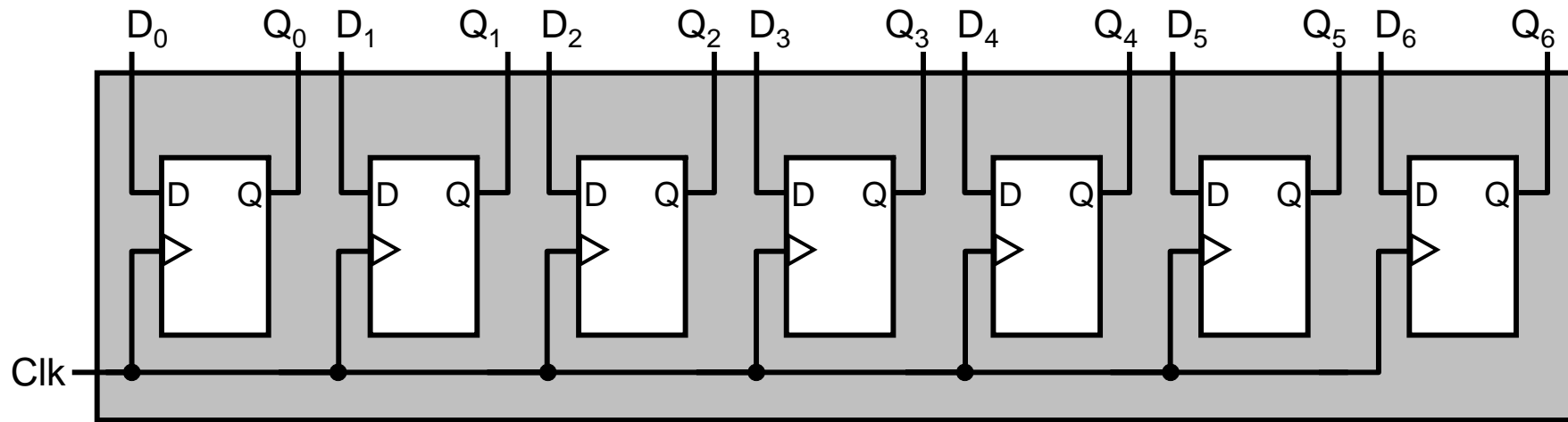
SISO Register
Serial-in, Serial-out

Shift Register Variants



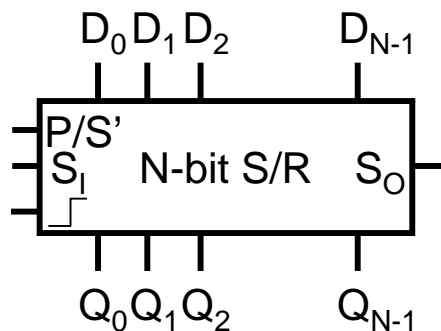
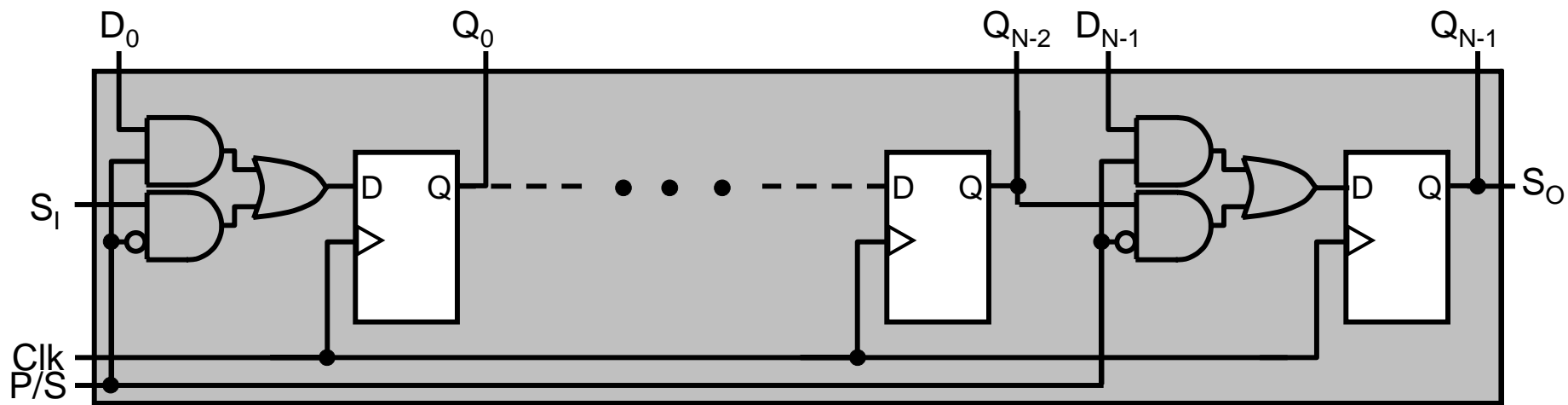
SIPO Register
Serial-in, Parallel-out

Shift Register Variants



PIPO Register
Parallel-in, Parallel-out

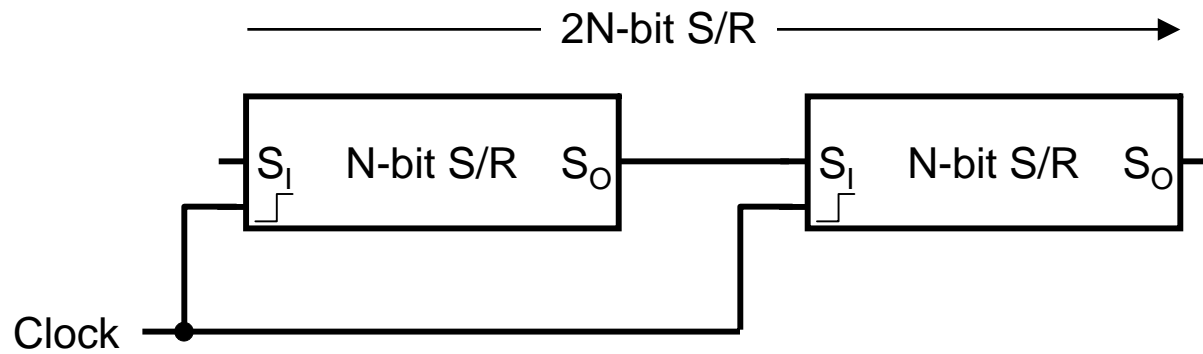
Shift Register Variants



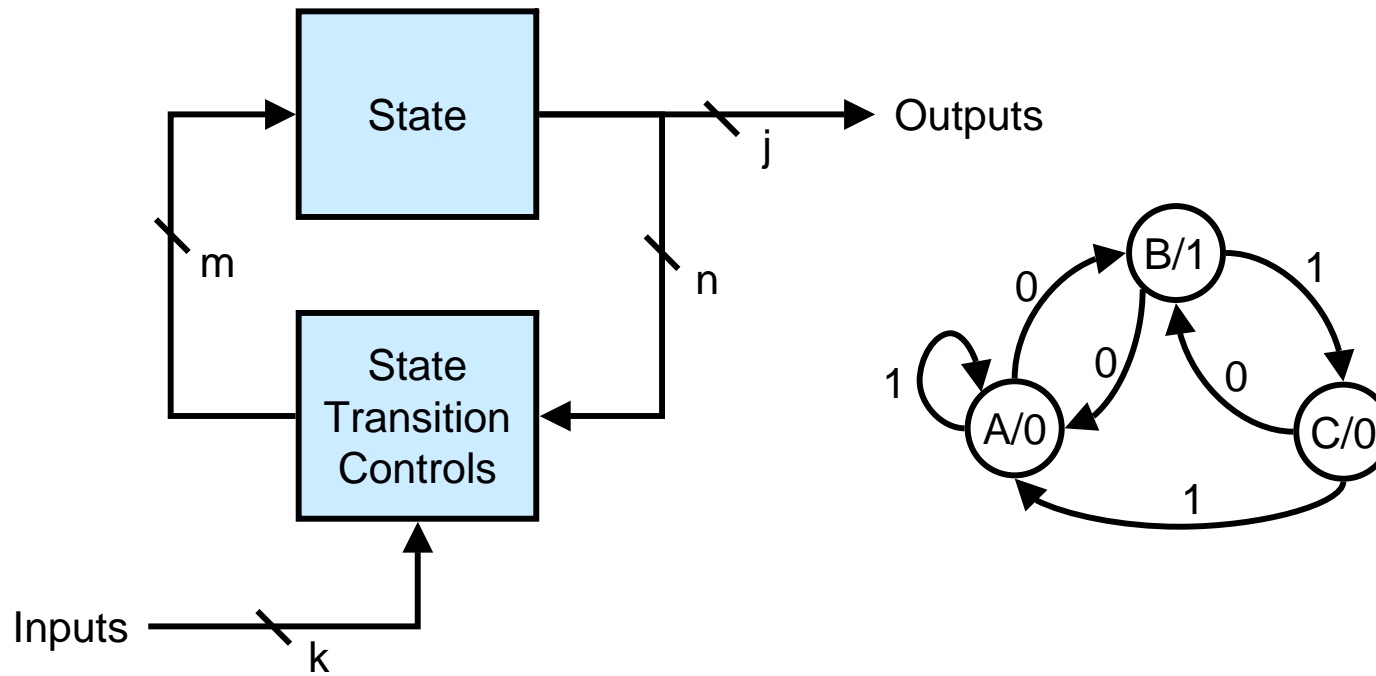
Serial/Parallel Register
 Parallel-in/Serial-in,
 Parallel-out/Serial-out

Tandem S/Rs

- Serial registers

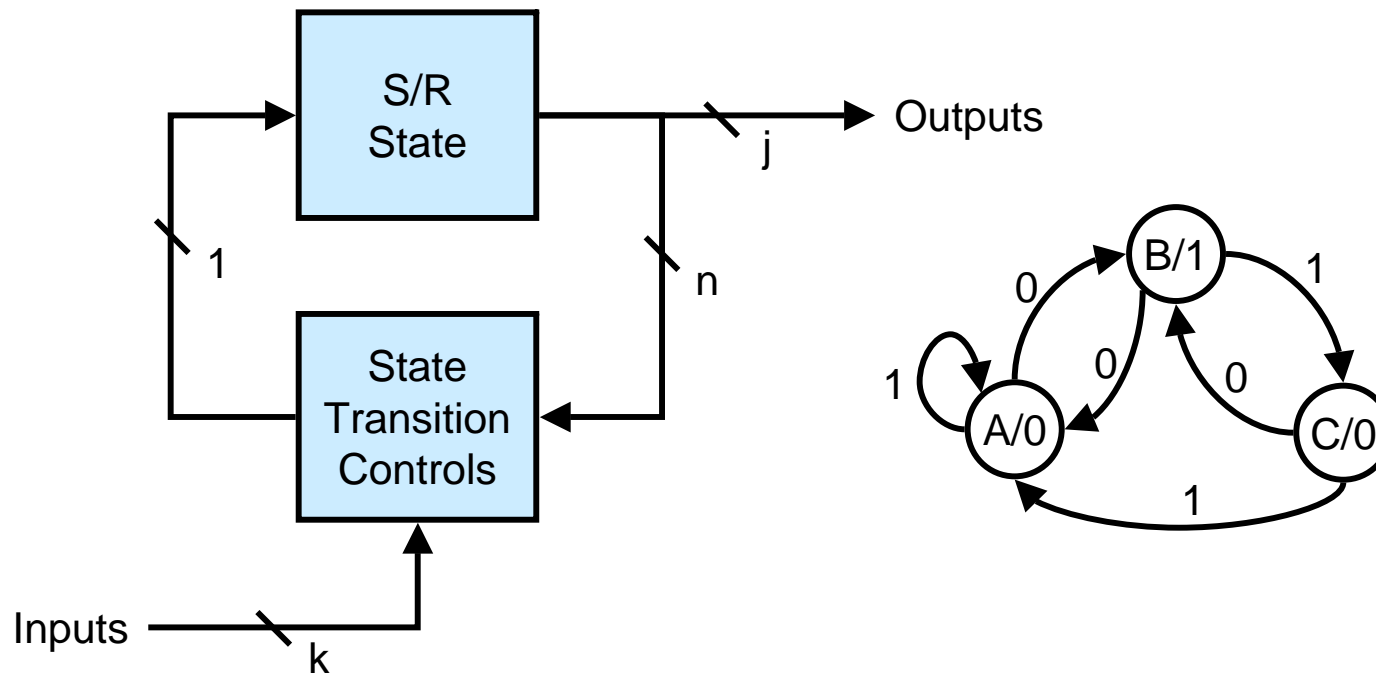


Generic Moore Machine



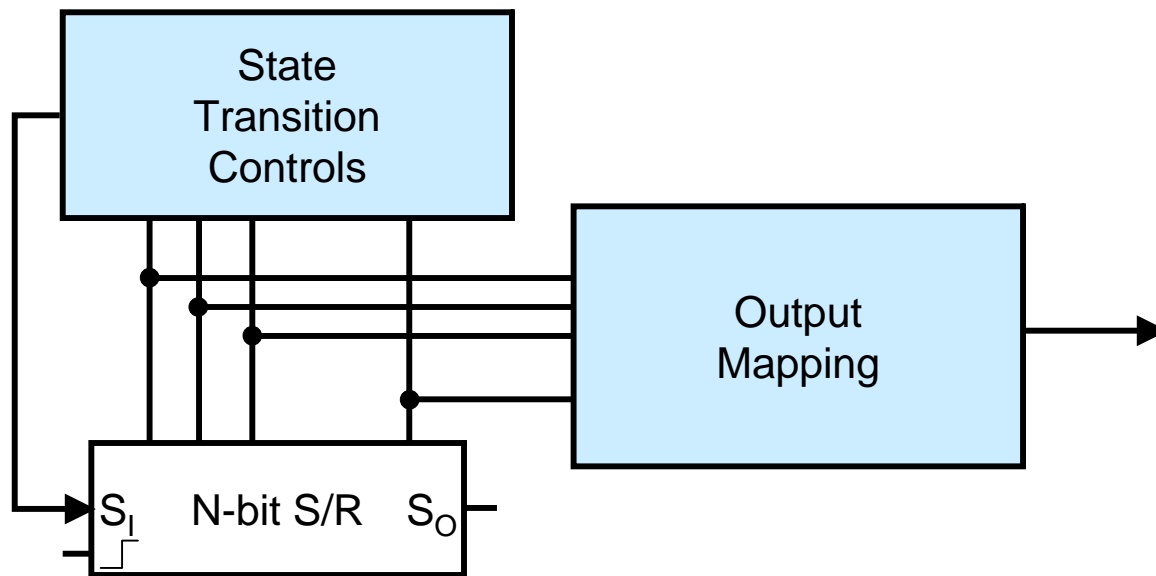
- All state-to-state transitions are potentially allowable.

S/R-based Moore Machine

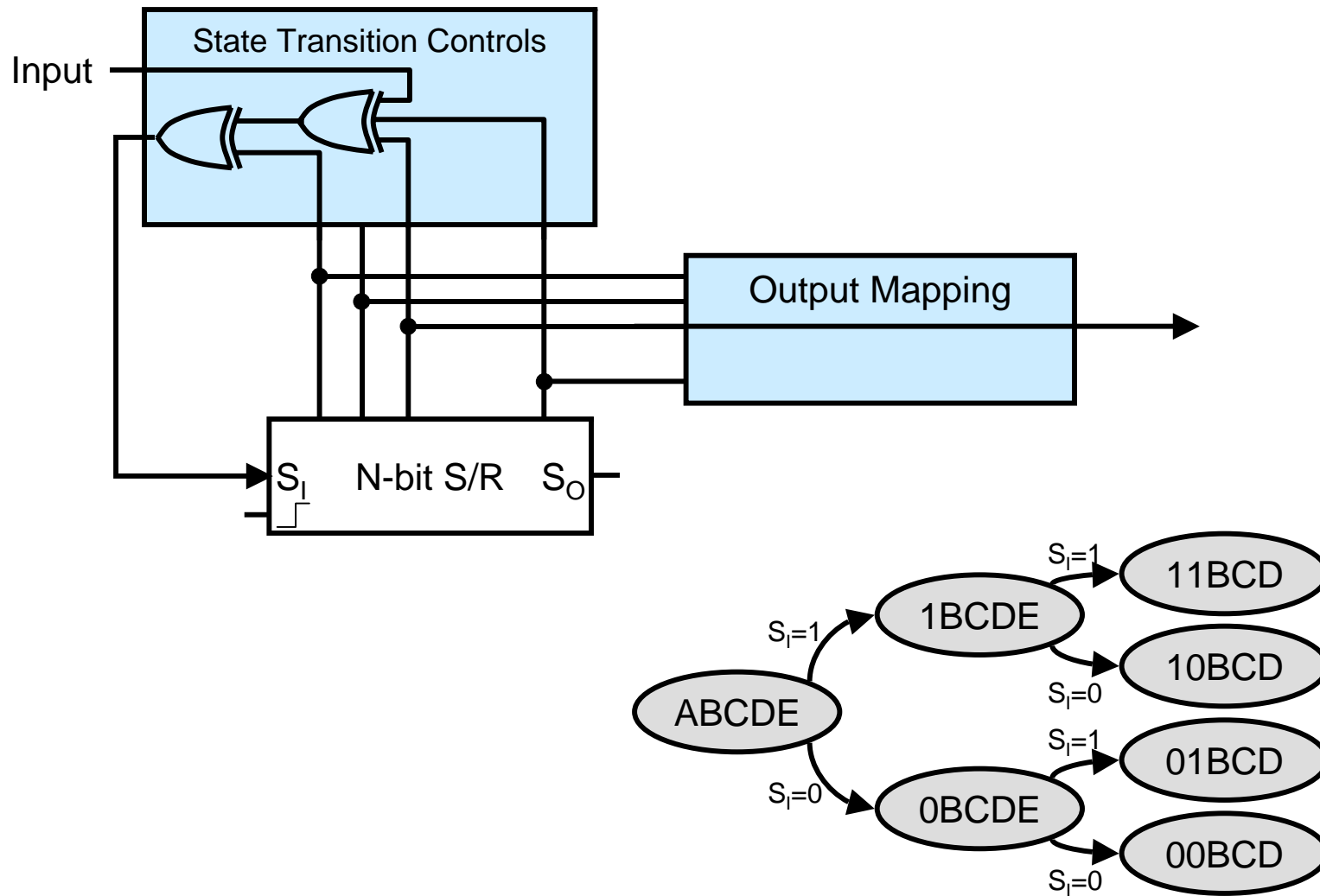


- Only specific state-to-state transitions are allowable.

Shift Register Sequences

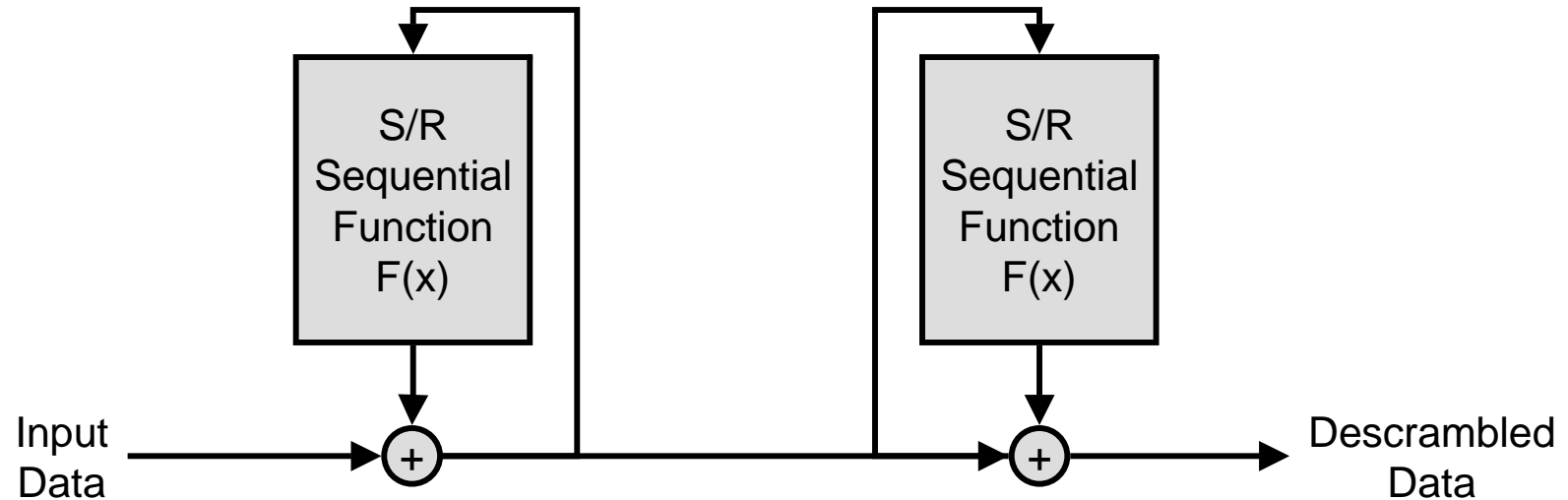


Shift Register Sequences



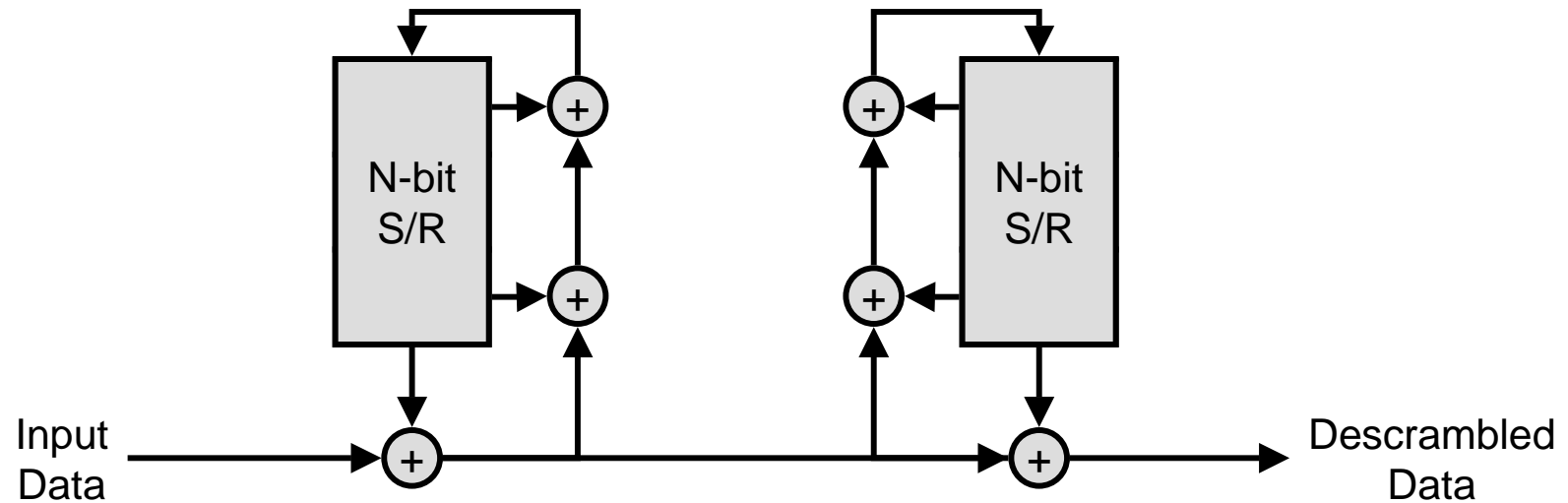
S/R Data Scrambler/Encryptor

- Fracasi scrambler:

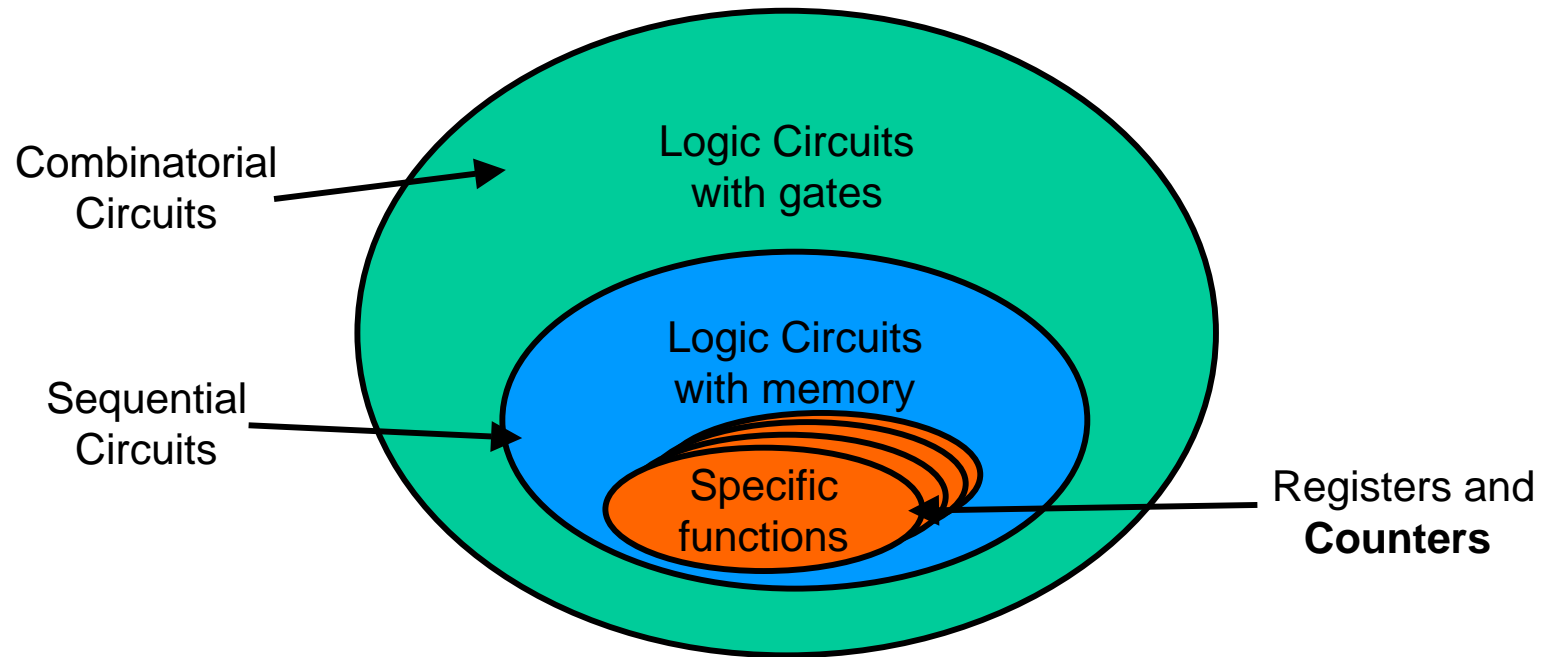


S/R Data Scrambler/Encryptor

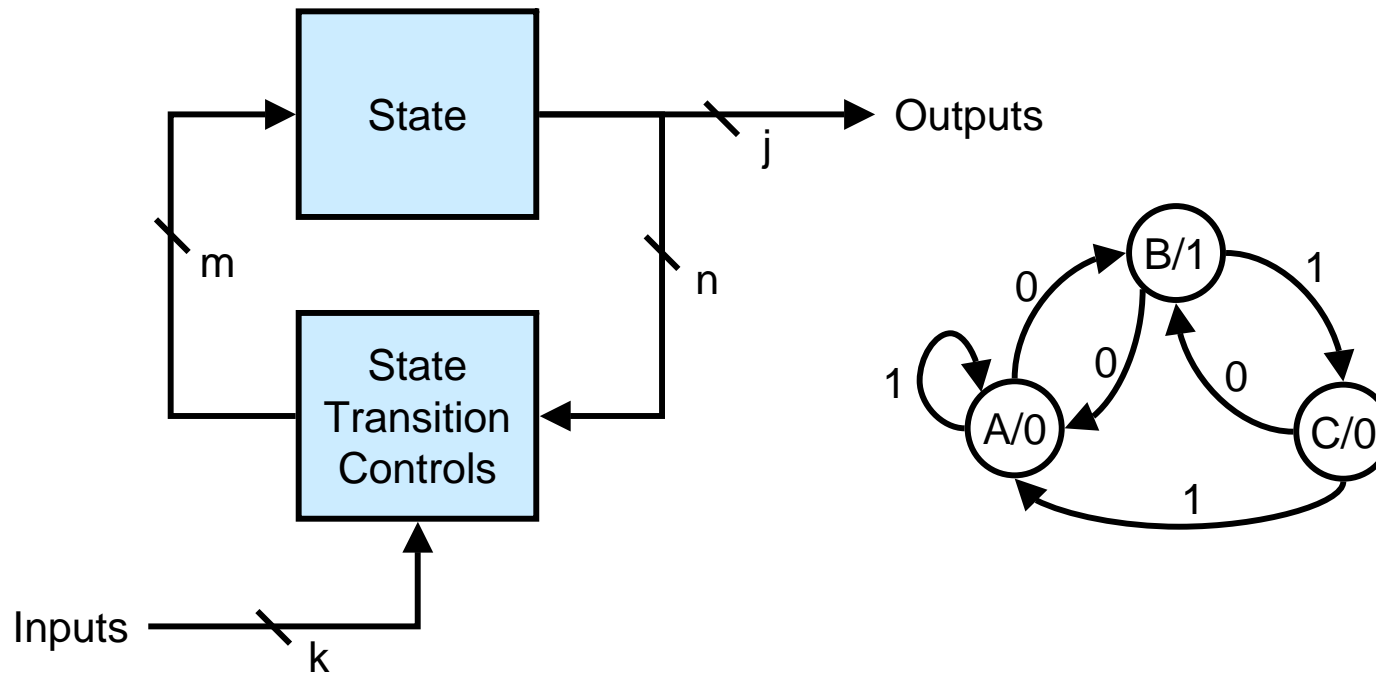
- Fraccassi scrambler:



Course Roadmap

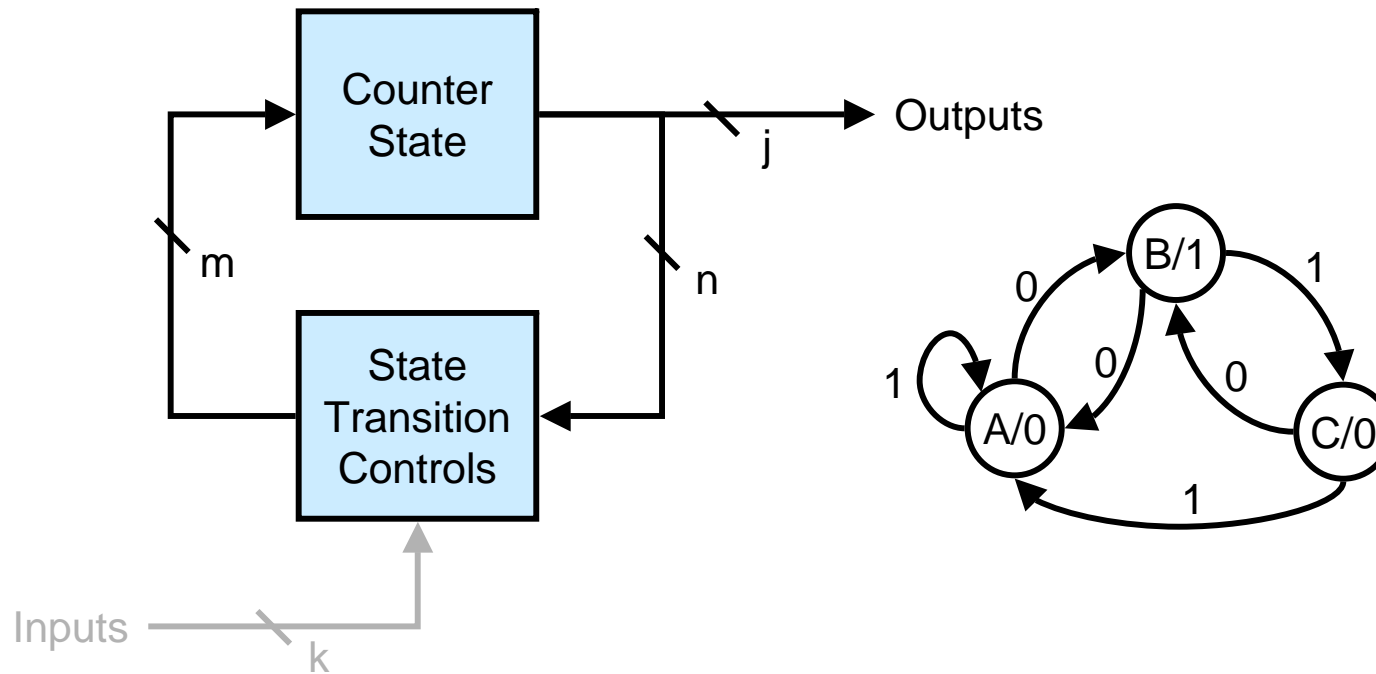


Generic Moore Machine



- All state-to-state transitions are potentially allowable.

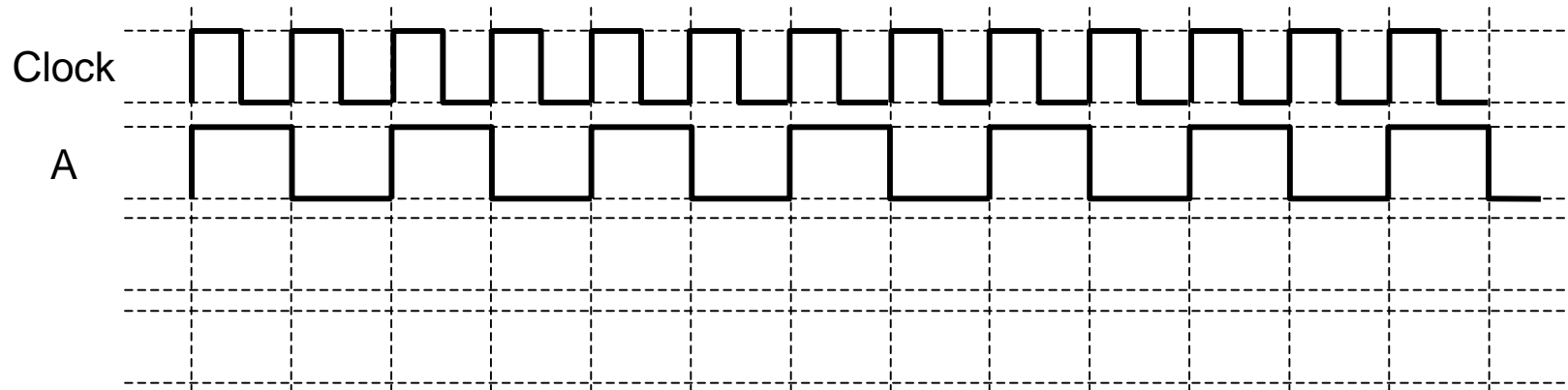
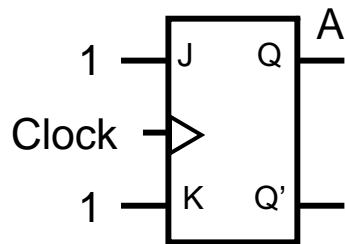
Counter Moore Machine



- State-to-state transitions follow a counting sequence
- Inputs (if any) may be used to set counting range, direction, starting point

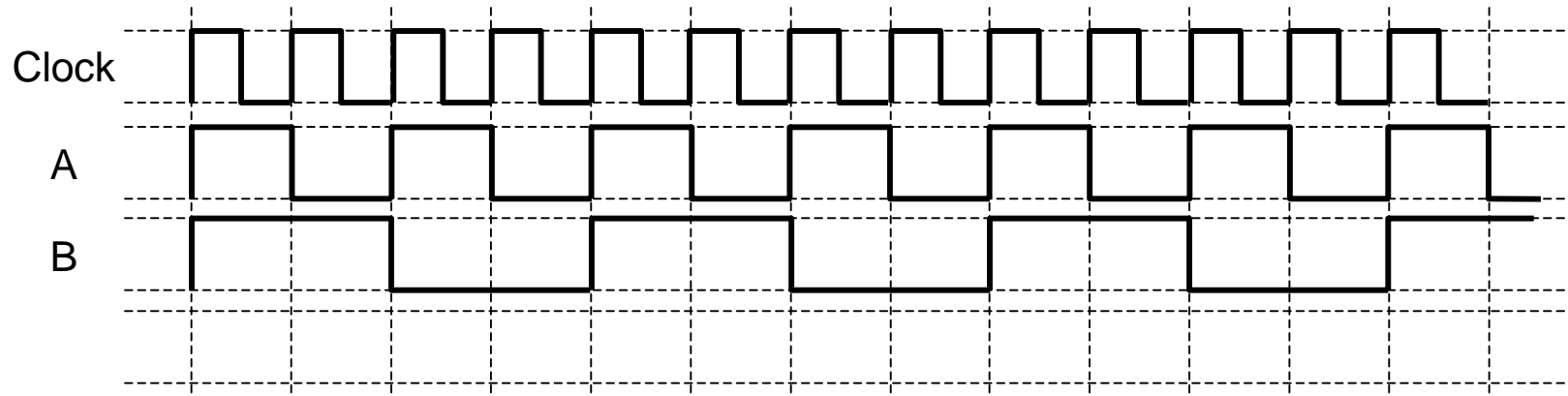
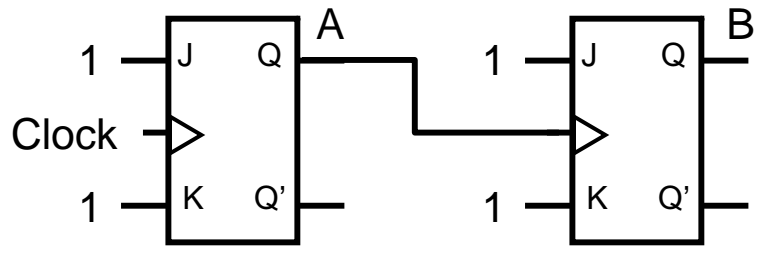
Counters

- Binary Ripple Counter



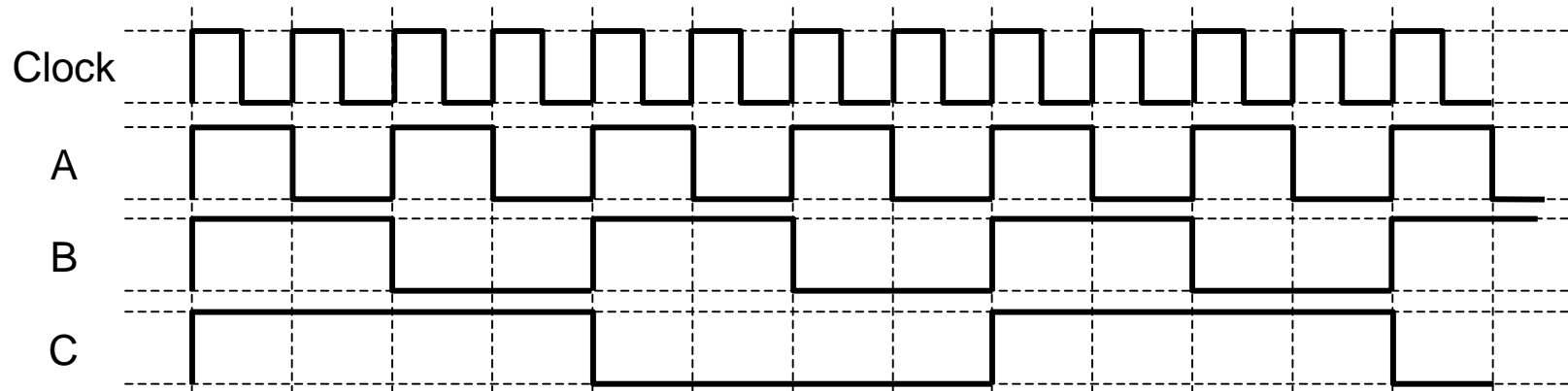
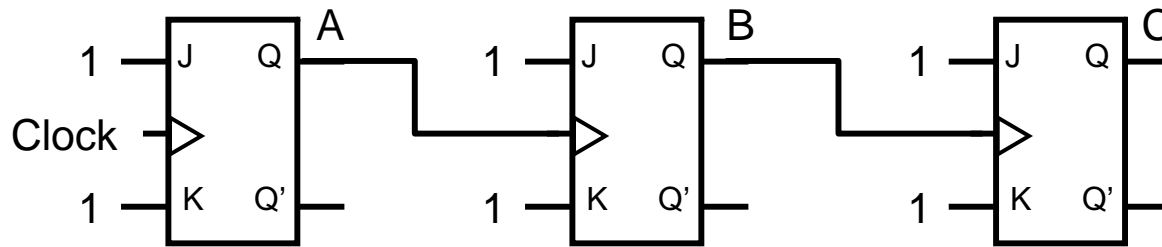
Counters

- Binary Ripple Counter



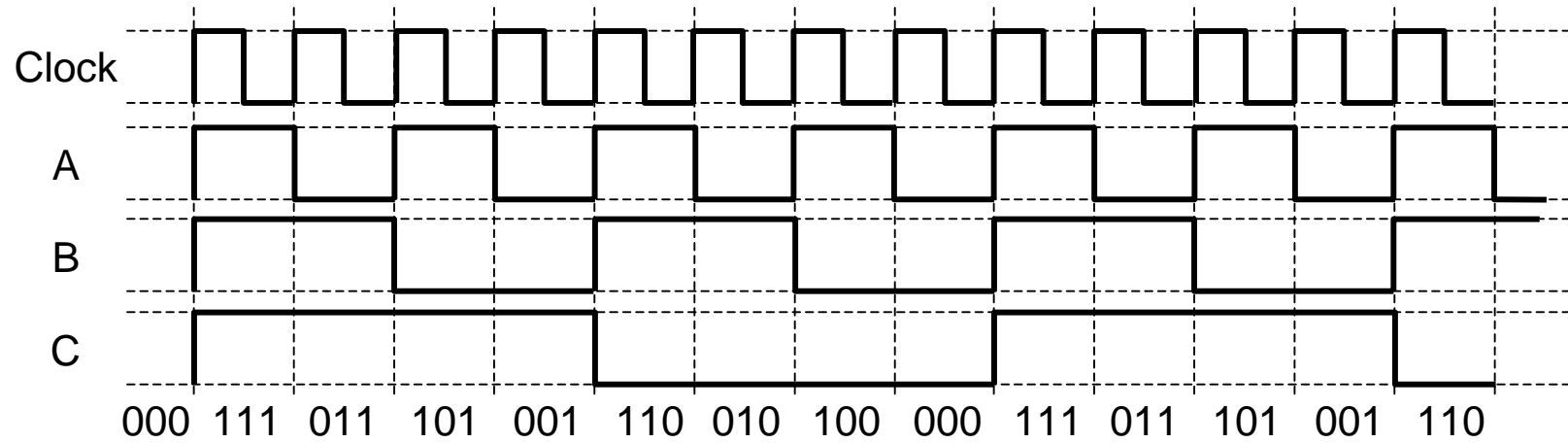
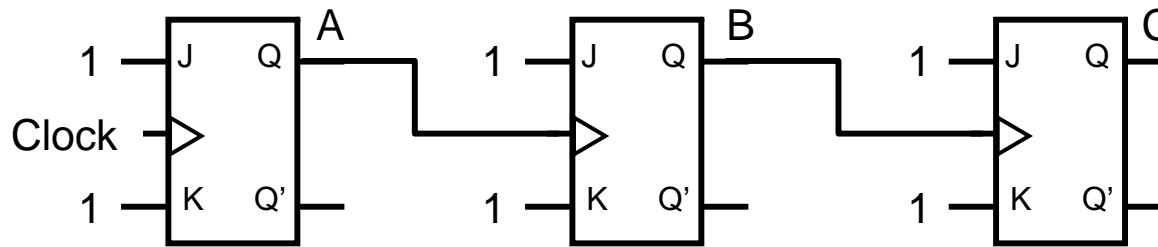
Counters

- Binary Ripple Counter



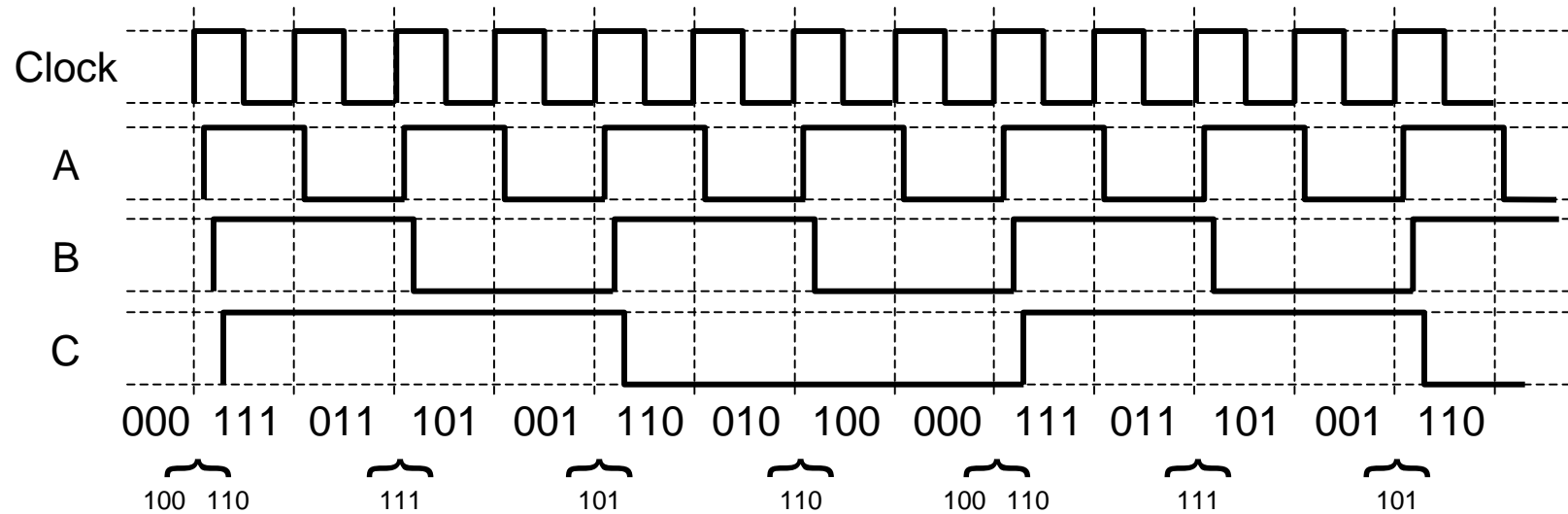
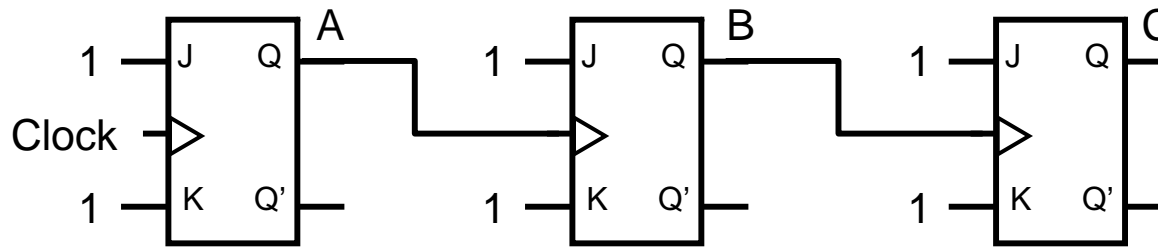
Counters

- Binary Ripple Counter (idealized)

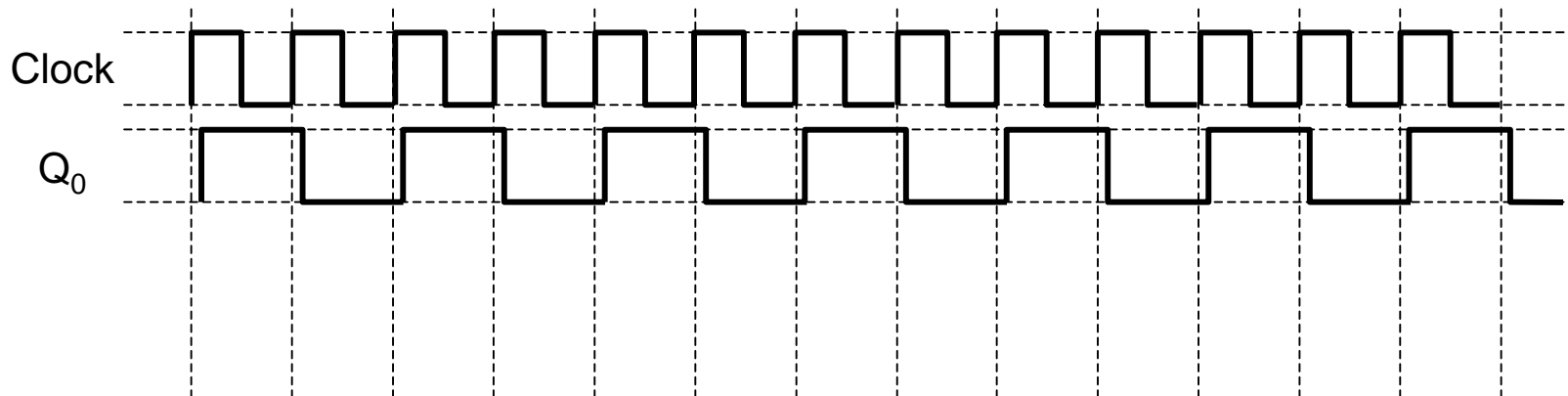
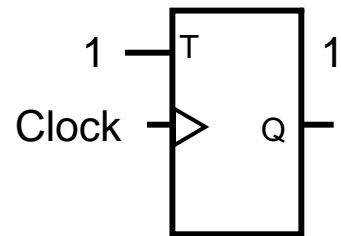


Counters

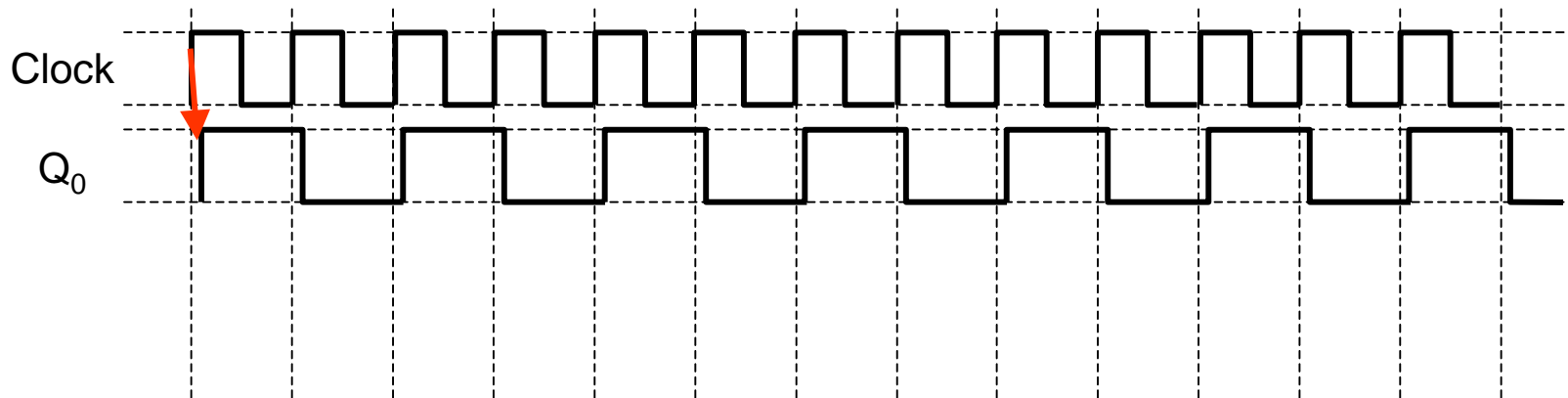
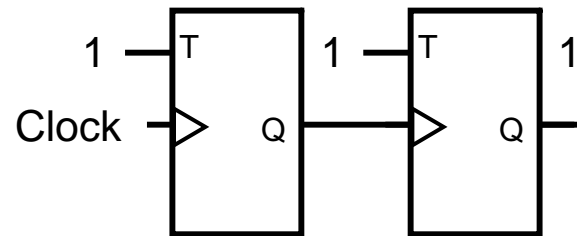
- Binary Ripple Counter (more realistic)



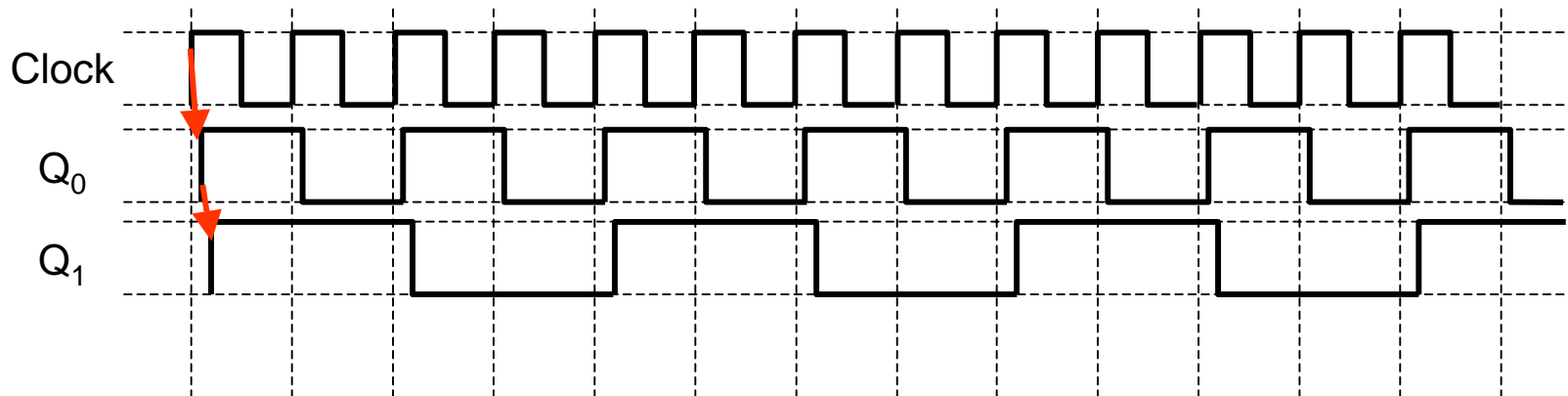
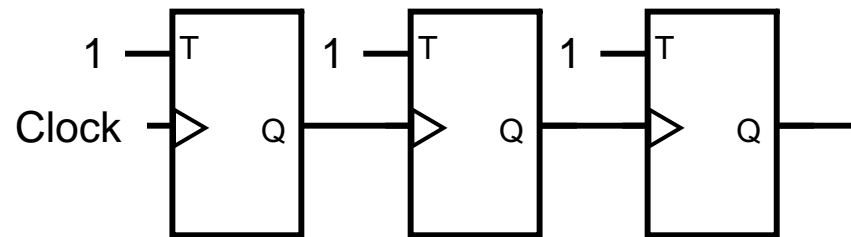
Cascading Counters



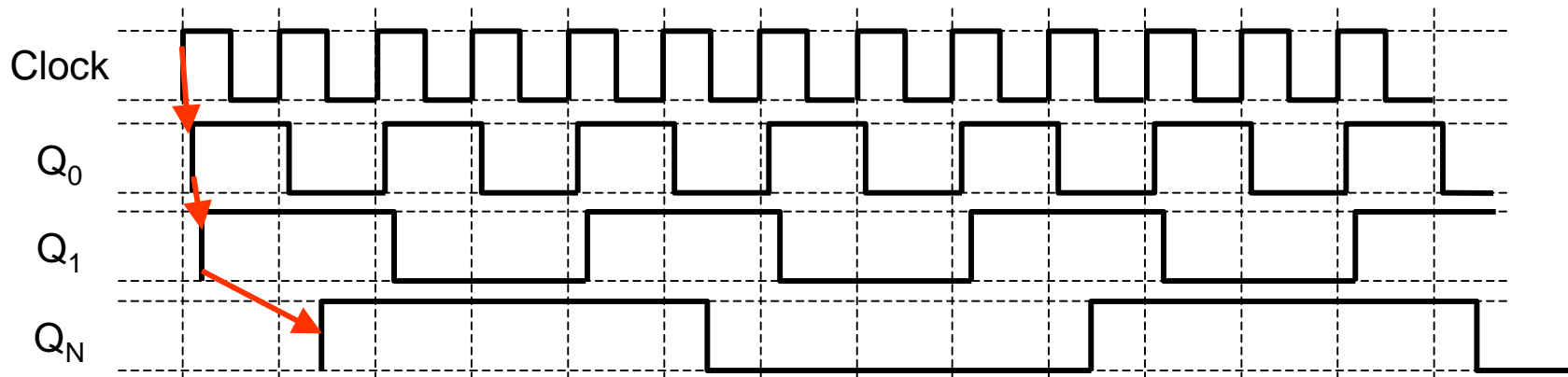
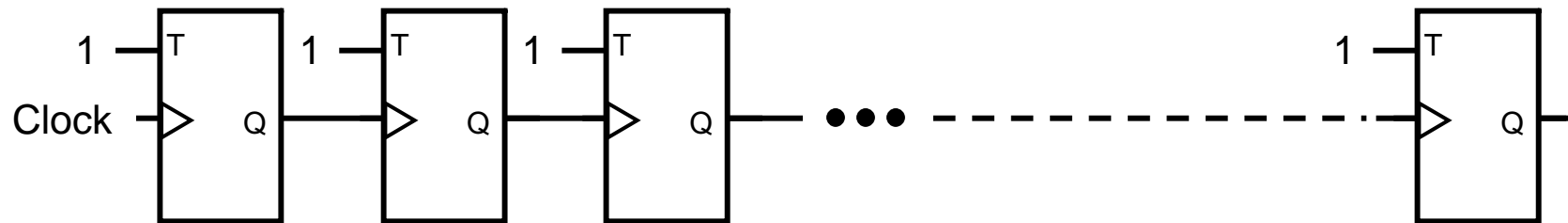
Cascading Counters



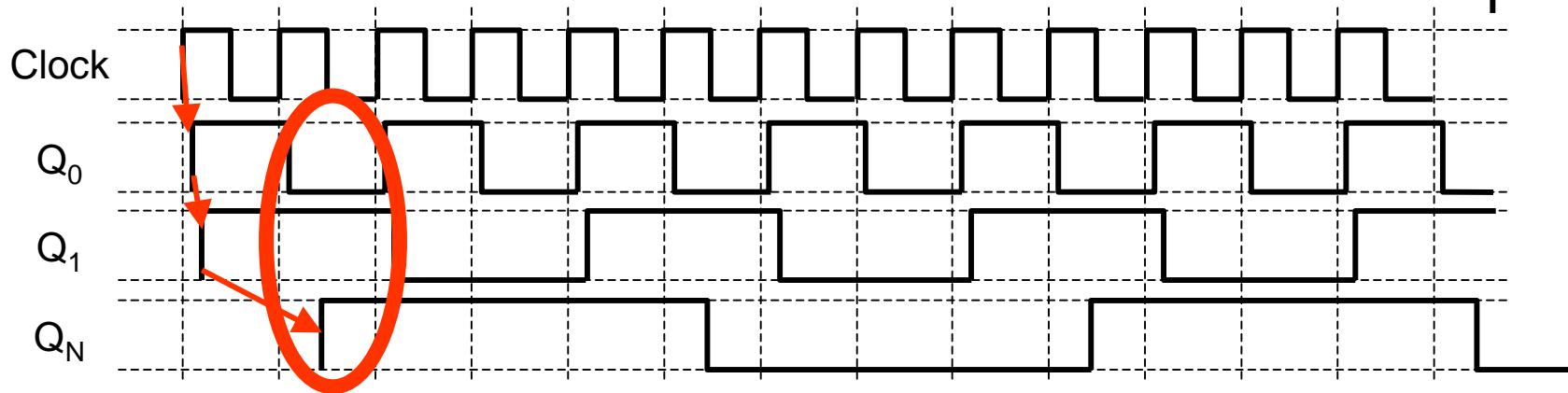
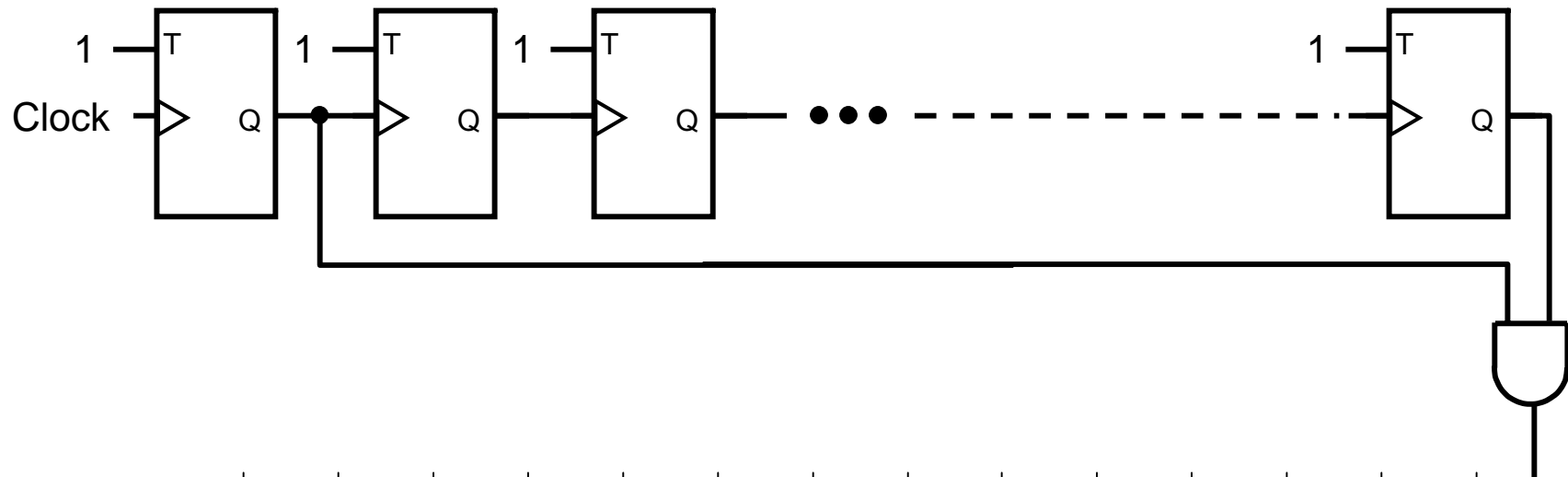
Cascading Counters



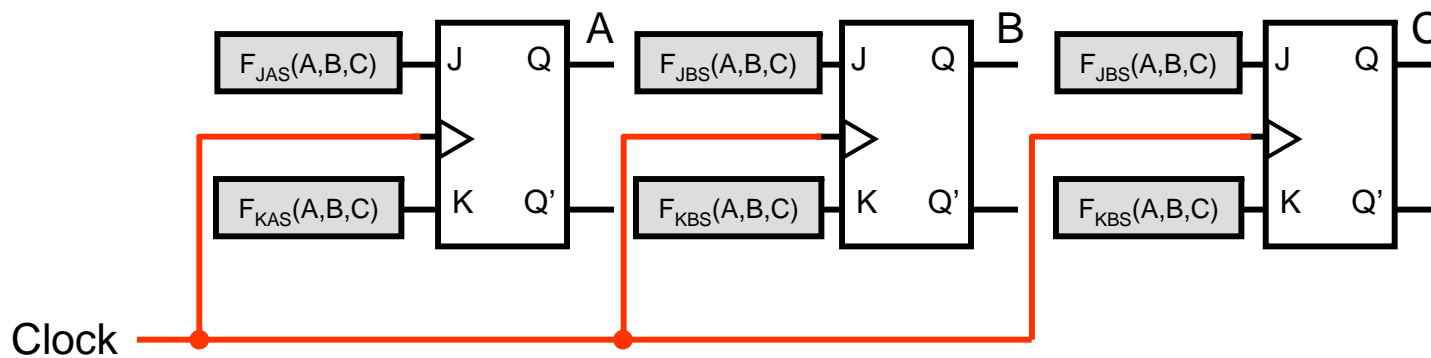
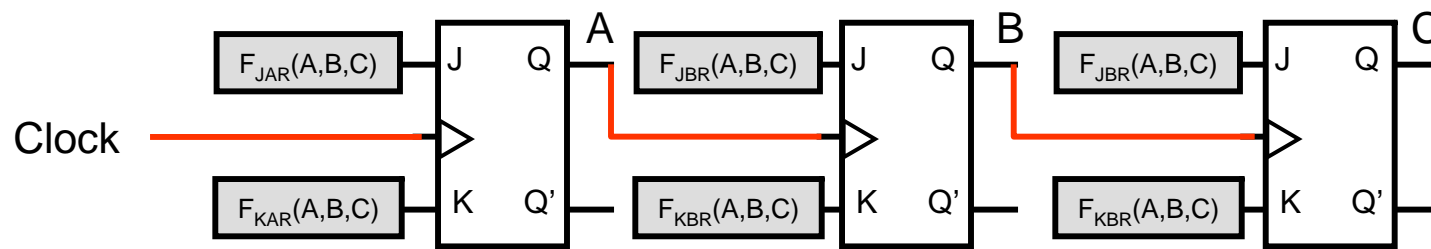
Cascading Counters



Cascading Counters



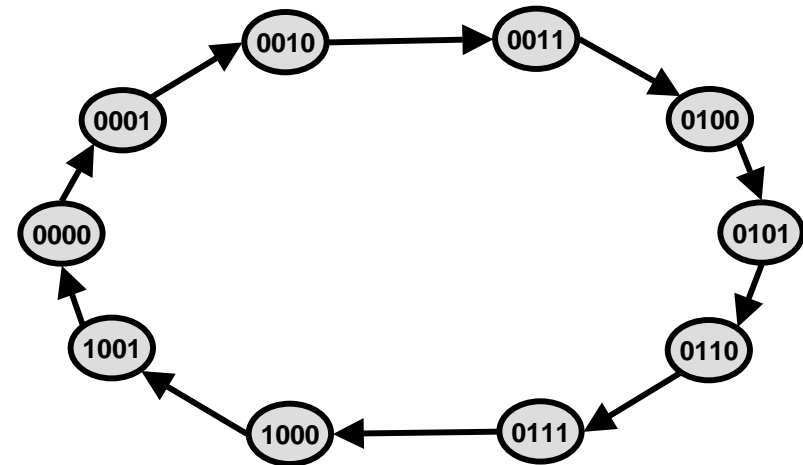
Ripple Counters vs. Synchronous Counters



Synchronous Counters

- BCD Counter:
State table

Present State	Next State
0000	0001
0001	0010
0010	0011
0011	0100
0100	0101
0101	0110
0110	0111
0111	1000
1000	1001
1001	0000

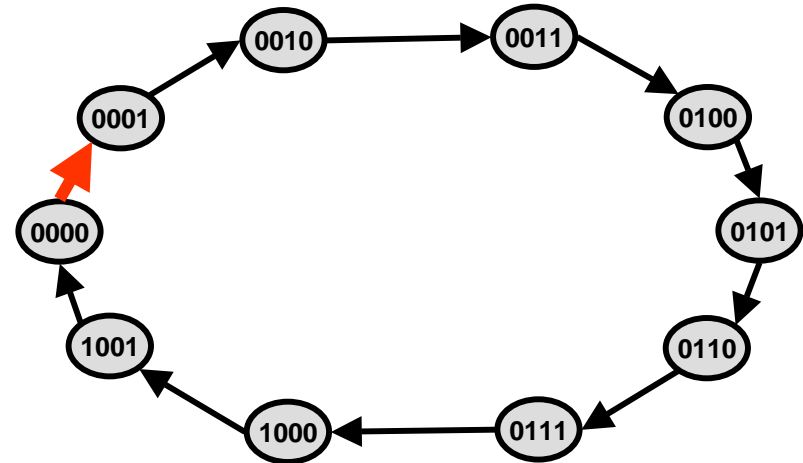


Synchronous Counters

• BCD Counter: J-K inputs

	DC	BA	00	01	11	10
J_A	00		1			
	01					
	11					
	10					
J_B	00		0			
	01					
	11					
	10					
J_C	00		0			
	01					
	11					
	10					
J_D	00		0			
	01					
	11					
	10					

	DC	BA	00	01	11	10
K_A	00		X			
	01					
	11					
	10					
K_B	00		X			
	01					
	11					
	10					
K_C	00		X			
	01					
	11					
	10					
K_D	00		X			
	01					
	11					
	10					



J-K operation:

$$0 \xrightarrow[0]{X} 0$$

$$0 \xrightarrow[1]{X} 1$$

$$1 \xrightarrow[1]{X} 0$$

$$1 \xrightarrow[0]{X} 1$$

Present State	Next State
0000	0001
0001	0010
0010	0011
0011	0100
0100	0101
0101	0110
0110	0111
0111	1000
1000	1001
1001	0000

Synchronous Counters

• BCD Counter: J-K inputs

DC	BA			
	00	01	11	10
00	1			
01				
11	X	X	X	X
10			X	X

J_A

DC	BA			
	00	01	11	10
00	0			
01				
11	X	X	X	X
10			X	X

J_B

DC	BA			
	00	01	11	10
00	0			
01				
11	X	X	X	X
10			X	X

J_C

DC	BA			
	00	01	11	10
00	0			
01				
11	X	X	X	X
10			X	X

J_D

DC	BA			
	00	01	11	10
00	X			
01				
11	X	X	X	X
10			X	X

K_A

DC	BA			
	00	01	11	10
00	X			
01				
11	X	X	X	X
10			X	X

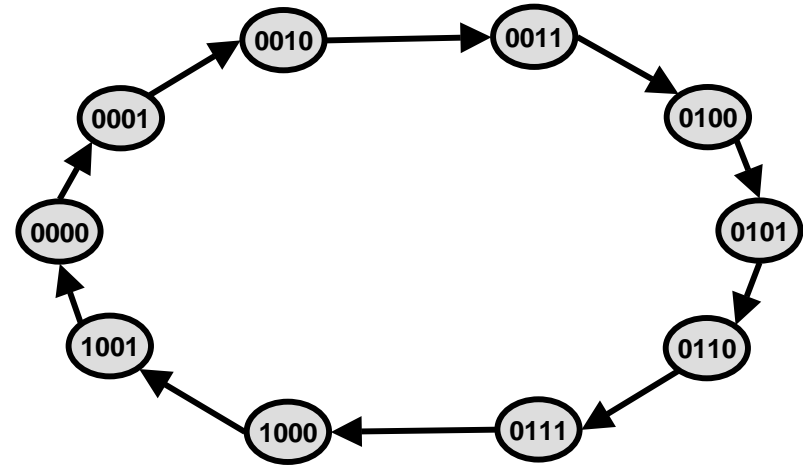
K_B

DC	BA			
	00	01	11	10
00	X			
01				
11	X	X	X	X
10			X	X

K_C

DC	BA			
	00	01	11	10
00	X			
01				
11	X	X	X	X
10			X	X

K_D



J-K operation:

$$0 \xrightarrow{0} 0$$

$$0 \xrightarrow{1} 1$$

$$1 \xrightarrow{1} 0$$

$$1 \xrightarrow{0} 1$$

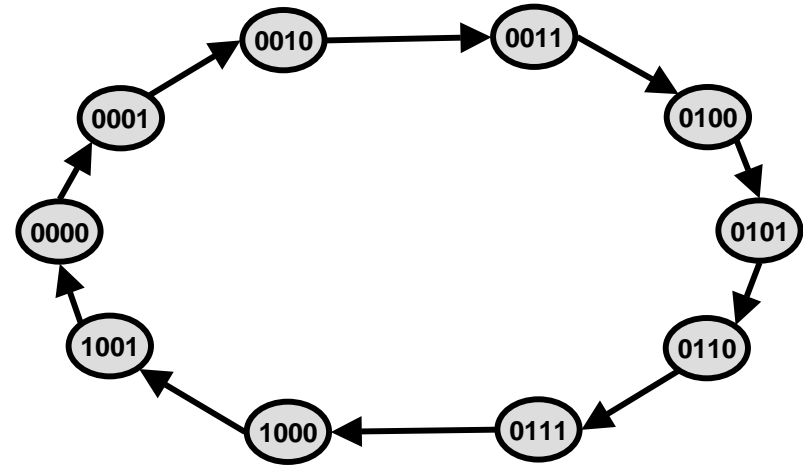
Present State	Next State
0000	0001
0001	0010
0010	0011
0011	0100
0100	0101
0101	0110
0110	0111
0111	1000
1000	1001
1001	0000

Synchronous Counters

• BCD Counter: J-K inputs

		BA			
		00	01	11	10
J _A	DC	1	X	X	1
	00	1	X	X	1
	01	X	X	X	X
	10	1	X	X	X
J _B	DC	0	1	X	X
	00	0	1	X	X
	01	X	X	X	X
	10	0	0	X	X
J _C	DC	0	0	1	0
	00	X	X	X	X
	01	X	X	X	X
	10	0	0	X	X
J _D	DC	0	0	0	0
	00	0	0	1	0
	01	X	X	X	X
	10	X	X	X	X

		BA			
		00	01	11	10
K _A	DC	X	1	1	X
	00	X	1	1	X
	01	X	X	X	X
	10	X	1	X	X
K _B	DC	X	X	1	0
	00	X	X	1	0
	01	X	X	X	X
	10	X	X	X	X
K _C	DC	X	X	X	X
	00	0	0	1	0
	01	X	X	X	X
	10	X	X	X	X
K _D	DC	X	X	X	X
	00	X	X	X	X
	01	X	X	X	X
	10	0	1	X	X



J-K operation:

$$0 \xrightarrow[0]{X} 0$$

$$0 \xrightarrow[1]{X} 1$$

$$1 \xrightarrow[1]{X} 0$$

$$1 \xrightarrow[0]{X} 1$$

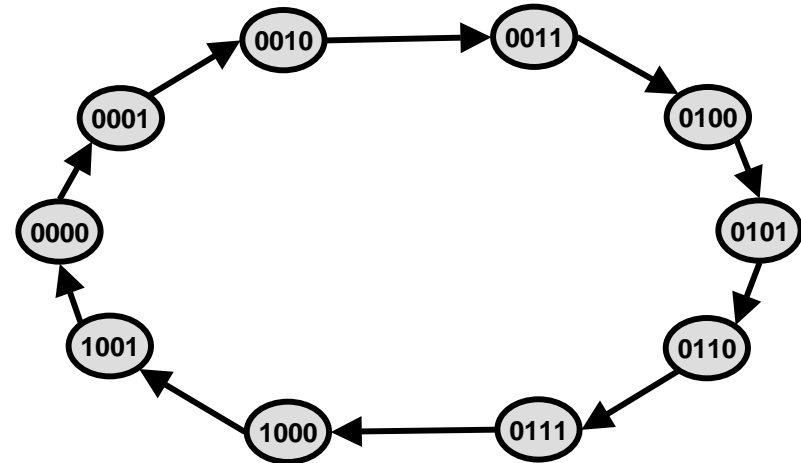
Present State	Next State
0000	0001
0001	0010
0010	0011
0011	0100
0100	0101
0101	0110
0110	0111
0111	1000
1000	1001
1001	0000

Synchronous Counters

• BCD Counter: J-K inputs

	DC	BA	00	01	11	10
J_A	00		1	X	X	1
	01		1	X	X	1
	11		X	X	X	X
	10		1	X	X	X
J_B	00		0	1	X	X
	01		0	1	X	X
	11		X	X	X	X
	10		0	0	X	X
J_C	00		0	0	1	0
	01		X	X	X	X
	11		X	X	X	X
	10		0	0	X	X
J_D	00		0	0	0	0
	01		0	0	1	0
	11		X	X	X	X
	10		X	X	X	X

	DC	BA	00	01	11	10
K_A	00		X	1	1	X
	01		X	1	1	X
	11		X	X	X	X
	10		X	1	X	X
K_B	00		X	X	1	0
	01		X	X	1	0
	11		X	X	X	X
	10		X	X	X	X
K_C	00		X	X	X	X
	01		0	0	1	0
	11		X	X	X	X
	10		X	X	X	X
K_D	00		X	X	X	X
	01		X	X	X	X
	11		X	X	X	X
	10		0	1	X	X



J-K operation:

$$0 \xrightarrow[0]{X} 0$$

$$0 \xrightarrow[1]{X} 1$$

$$1 \xrightarrow[0]{X} 0$$

$$1 \xrightarrow[1]{X} 1$$

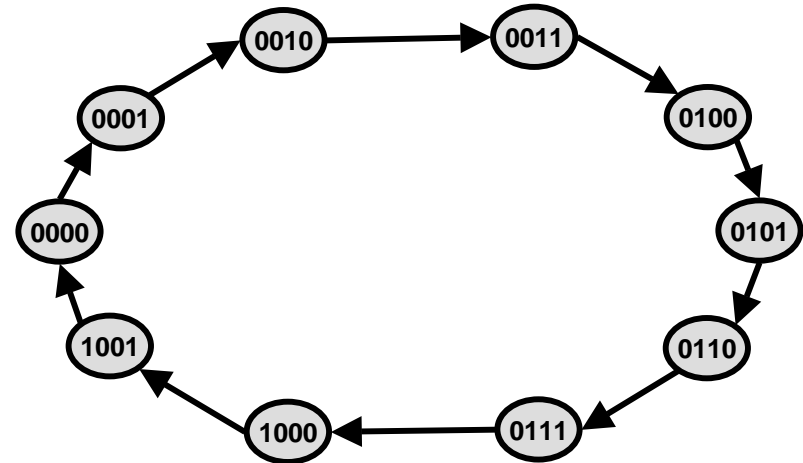
Present State	Next State
0000	0001
0001	0010
0010	0011
0011	0100
0100	0101
0101	0110
0110	0111
0111	1000
1000	1001
1001	0000

Synchronous Counters

• BCD Counter: J-K inputs

		BA			
DC		00	01	11	10
J_A	00	1	X	X	1
	01	1	X	X	1
	11	X	X	X	X
	10	1	X	X	X
J_B	00	0	1	X	X
	01	0	1	X	X
	11	X	X	X	X
	10	0	0	X	X
J_C	00	0	0	1	0
	01	X	X	X	X
	11	X	X	X	X
	10	0	0	X	X
J_D	00	0	0	0	0
	01	0	0	1	0
	11	X	X	X	X
	10	X	X	X	X

		BA			
DC		00	01	11	10
K_A	00	X	1	1	X
	01	X	1	1	X
	11	X	X	X	X
	10	X	1	X	X
K_B	00	X	X	1	0
	01	X	X	1	0
	11	X	X	X	X
	10	X	X	X	X
K_C	00	X	X	X	X
	01	0	0	1	0
	11	X	X	X	X
	10	X	X	X	X
K_D	00	X	X	X	X
	01	X	X	X	X
	11	X	X	X	X
	10	0	1	X	X



$$J_A = 1$$

$$K_A = 1$$

$$J_B = AD'$$

$$K_B = A$$

$$J_C = AB$$

$$K_C = AB$$

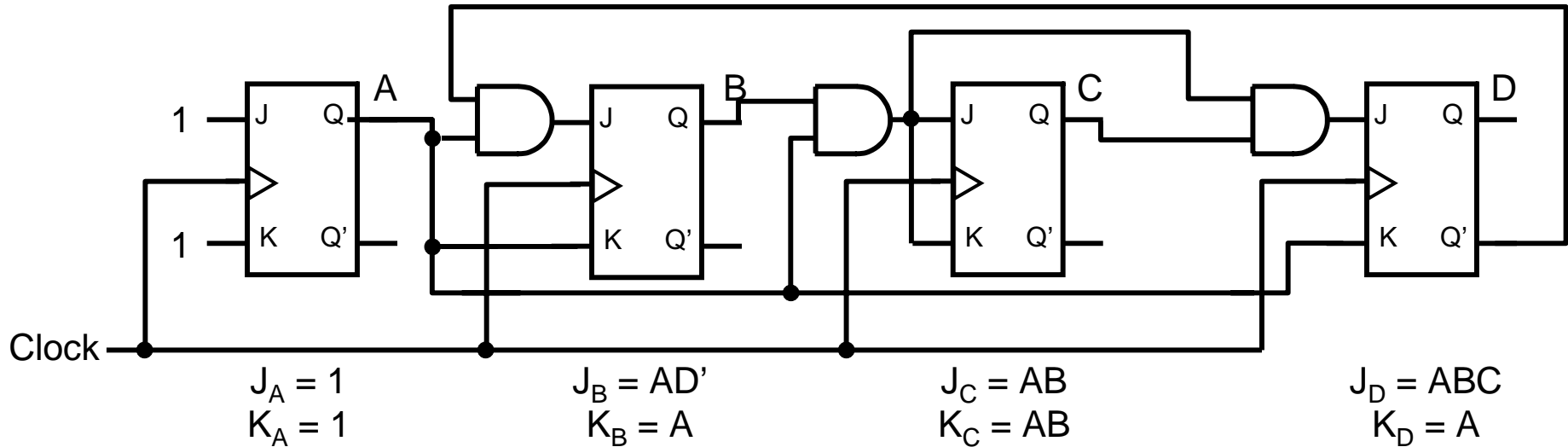
$$J_D = ABC$$

$$K_D = A$$

Present State	Next State
0000	0001
0001	0010
0010	0011
0011	0100
0100	0101
0101	0110
0110	0111
0111	1000
1000	1001
1001	0000

Synchronous Counters

- BCD Counter



Present State	$J_D K_D$	$J_C K_C$	$J_B K_B$	$J_A K_A$	Next State
0000	00	00	00	11	0001
0001	01	00	11	11	0010
0010	00	00	00	11	0011
0011	01	11	11	11	0100
0100	00	00	00	11	0101
0101	01	00	11	11	0110
0110	00	00	00	11	0111
0111	11	11	11	11	1000

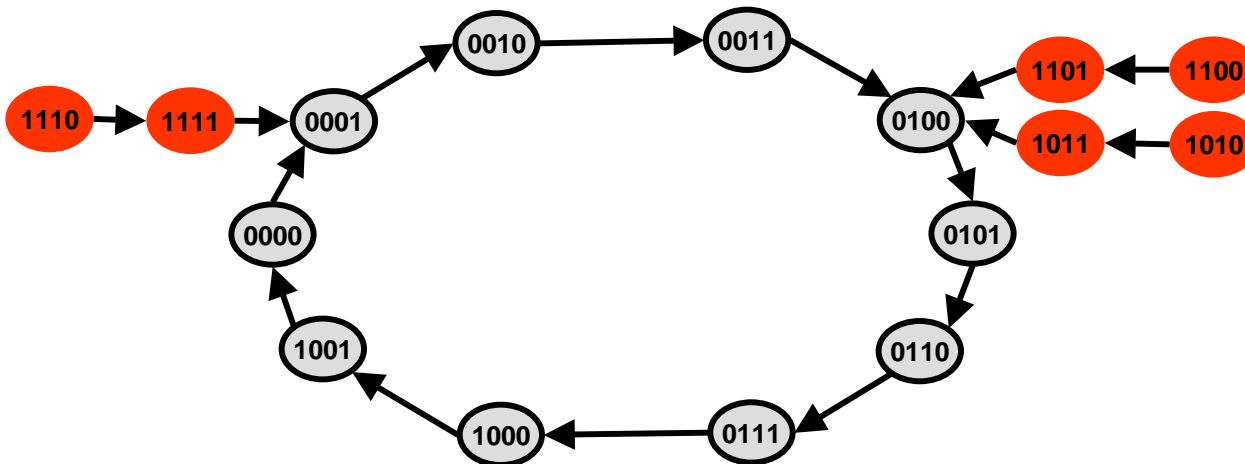
Present State	$J_D K_D$	$J_C K_C$	$J_B K_B$	$J_A K_A$	Next State
1000	00	00	00	11	1001
1001	01	00	01	11	0000
1010	00	00	00	11	1011
1011	01	11	01	11	0100
1100	00	00	00	11	1101
1101	01	00	01	11	0100
1110	00	00	00	11	1111
1111	11	11	01	11	0001

Synchronous Counters

•BCD Counter

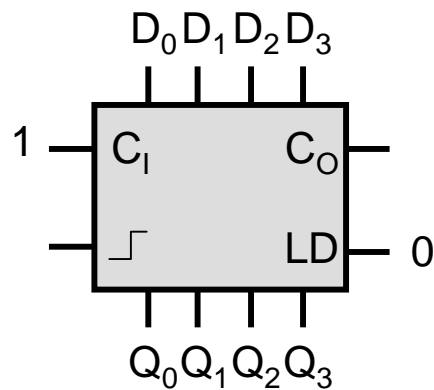
Present State	J _D K _D	J _C K _C	J _B K _B	J _A K _A	Next State
0000	00	00	00	11	0001
0001	01	00	11	11	0010
0010	00	00	00	11	0011
0011	01	11	11	11	0100
0100	00	00	00	11	0101
0101	01	00	11	11	0110
0110	00	00	00	11	0111
0111	11	11	11	11	1000

Present State	J _D K _D	J _C K _C	J _B K _B	J _A K _A	Next State
1000	00	00	00	11	1001
1001	01	00	01	11	0000
1010	00	00	00	11	1011
1011	01	11	01	11	0100
1100	00	00	00	11	1101
1101	01	00	01	11	0100
1110	00	00	00	11	1111
1111	11	11	01	11	0001



Varieties of Counters

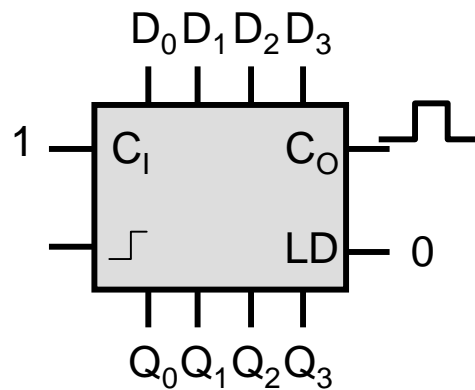
- Counters with Parallel Load
Normal counter operation



State	Load	C ₁	D ₃ D ₂ D ₁ D ₀	Next State	C ₀
0000	0	1	XXXX	0001	0
0001	0	1	XXXX	0010	0
0010	0	1	XXXX	0011	0
0011	0	1	XXXX	0100	0
0100	0	1	XXXX	1000	0
1000	0	1	XXXX	1001	0
1001	0	1	XXXX	1010	0
1010	0	1	XXXX	1011	0
1011	0	1	XXXX	1100	0
1100	0	1	XXXX	1101	0
1101	0	1	XXXX	1110	0
1110	0	1	XXXX	1111	0
1111	0	1	XXXX	0000	1
XXXX	1	X	ABCD	ABCD	0
WXYZ	0	0	XXXX	WXYZ	0

Varieties of Counters

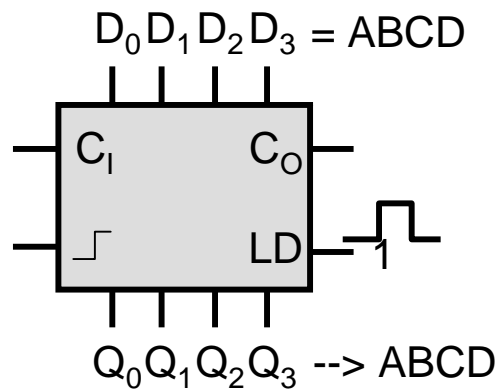
- Counters with Parallel Load
Normal counter operation



State	Load	C _i	D ₃ D ₂ D ₁ D ₀	Next State	C _o
0000	0	1	XXXX	0001	0
0001	0	1	XXXX	0010	0
0010	0	1	XXXX	0011	0
0011	0	1	XXXX	0100	0
0100	0	1	XXXX	1000	0
1000	0	1	XXXX	1001	0
1001	0	1	XXXX	1010	0
1010	0	1	XXXX	1011	0
1011	0	1	XXXX	1100	0
1100	0	1	XXXX	1101	0
1101	0	1	XXXX	1110	0
1110	0	1	XXXX	1111	0
1111	0	1	XXXX	0000	1
XXXX	1	X	ABCD	ABCD	0
WXYZ	0	0	XXXX	WXYZ	0

Varieties of Counters

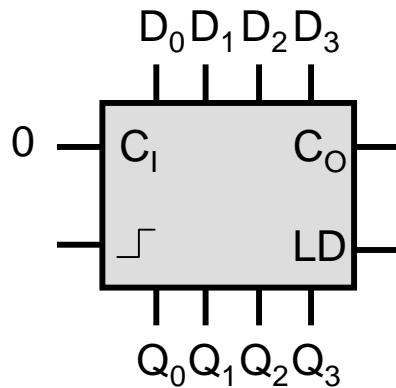
- Counters with Parallel Load
Loading next state in parallel



State	Load	C_1	$D_3D_2D_1D_0$	Next State	C_0
0000	0	1	XXXX	0001	0
0001	0	1	XXXX	0010	0
0010	0	1	XXXX	0011	0
0011	0	1	XXXX	0100	0
0100	0	1	XXXX	1000	0
1000	0	1	XXXX	1001	0
1001	0	1	XXXX	1010	0
1010	0	1	XXXX	1011	0
1011	0	1	XXXX	1100	0
1100	0	1	XXXX	1101	0
1101	0	1	XXXX	1110	0
1110	0	1	XXXX	1111	0
1111	0	1	XXXX	0000	1
XXXX	1	X	ABCD	ABCD	0
WXYZ	0	0	XXXX	WXYZ	0

Varieties of Counters

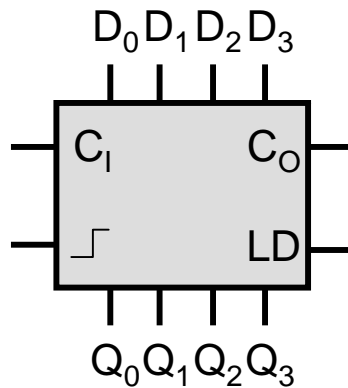
- Counters with Parallel Load



State	Load	C ₁	D ₃ D ₂ D ₁ D ₀	Next State	C ₀
0000	0	1	XXXX	0001	0
0001	0	1	XXXX	0010	0
0010	0	1	XXXX	0011	0
0011	0	1	XXXX	0100	0
0100	0	1	XXXX	1000	0
1000	0	1	XXXX	1001	0
1001	0	1	XXXX	1010	0
1010	0	1	XXXX	1011	0
1011	0	1	XXXX	1100	0
1100	0	1	XXXX	1101	0
1101	0	1	XXXX	1110	0
1110	0	1	XXXX	1111	0
1111	0	1	XXXX	0000	1
XXXX	1	X	ABCD	ABCD	0
WXYZ	0	0	XXXX	WXYZ	0

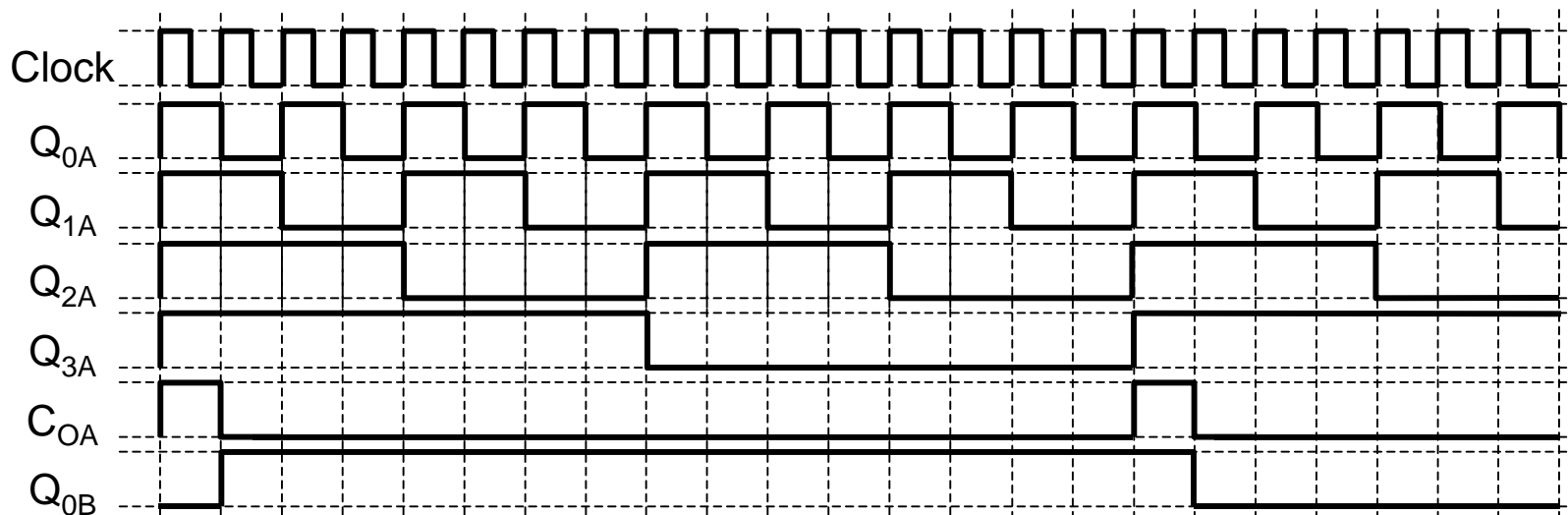
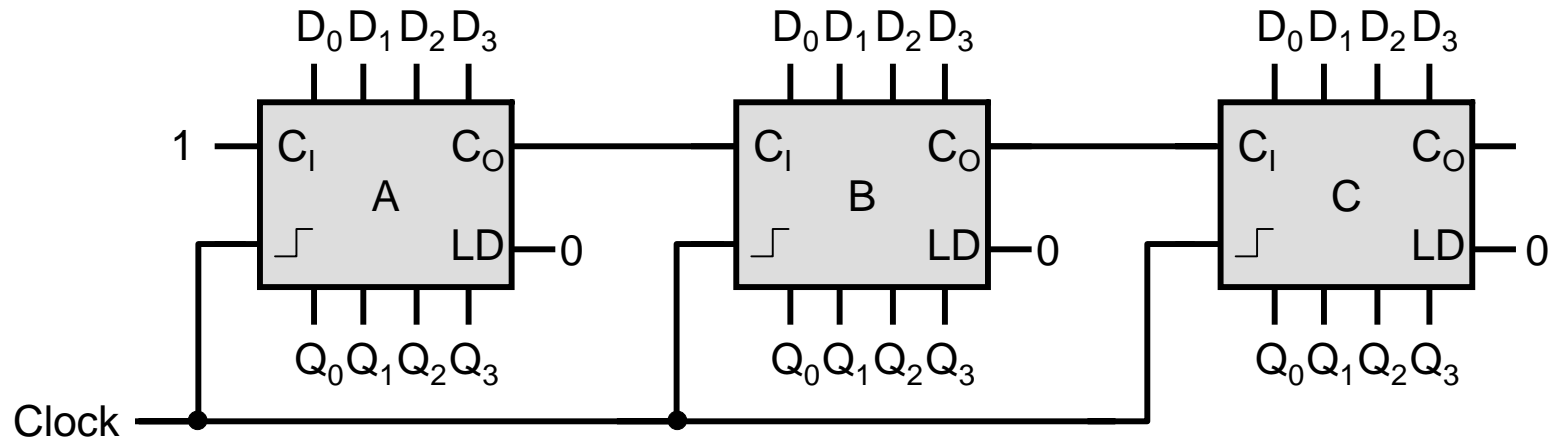
Varieties of Counters

- Counters with Parallel Load

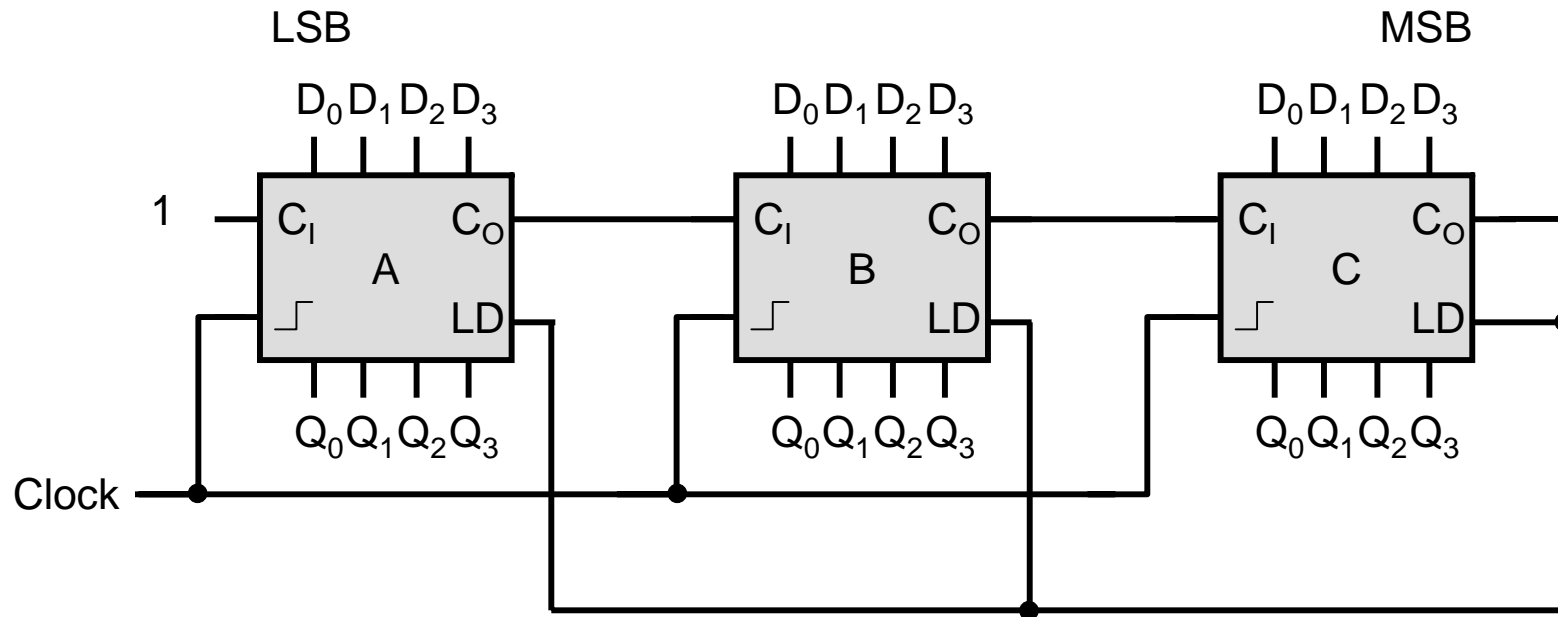


State	Load	C ₁	D ₃ D ₂ D ₁ D ₀	Next State	C ₀
0000	0	1	XXXX	0001	0
0001	0	1	XXXX	0010	0
0010	0	1	XXXX	0011	0
0011	0	1	XXXX	0100	0
0100	0	1	XXXX	1000	0
1000	0	1	XXXX	1001	0
1001	0	1	XXXX	1010	0
1010	0	1	XXXX	1011	0
1011	0	1	XXXX	1100	0
1100	0	1	XXXX	1101	0
1101	0	1	XXXX	1110	0
1110	0	1	XXXX	1111	0
1111	0	1	XXXX	0000	1
XXXX	1	X	ABCD	ABCD	0
WXYZ	0	0	XXXX	WXYZ	0

Cascading Synchronous Counters



Programmable Synchronous Counters

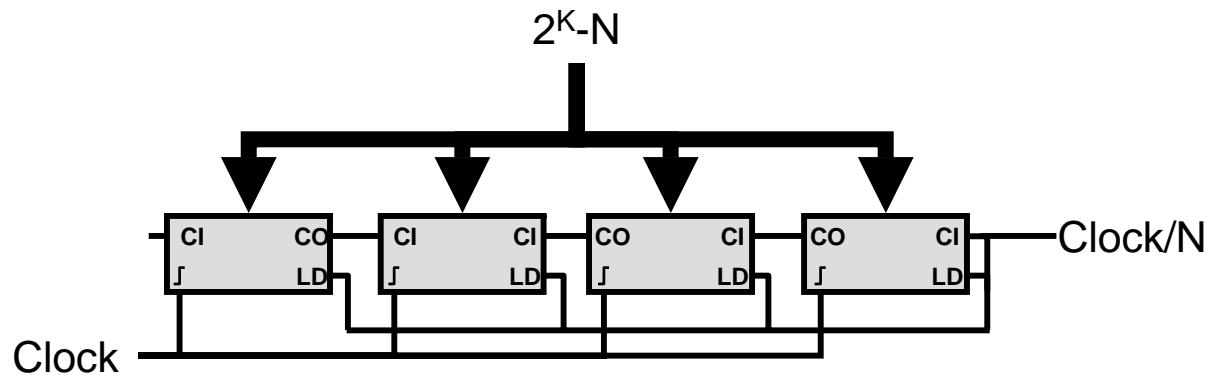


Assume $D_{3C} \dots D_{0A} = b_{11}b_{10}b_9b_8b_7b_6b_5b_4b_3b_2b_1b_0$

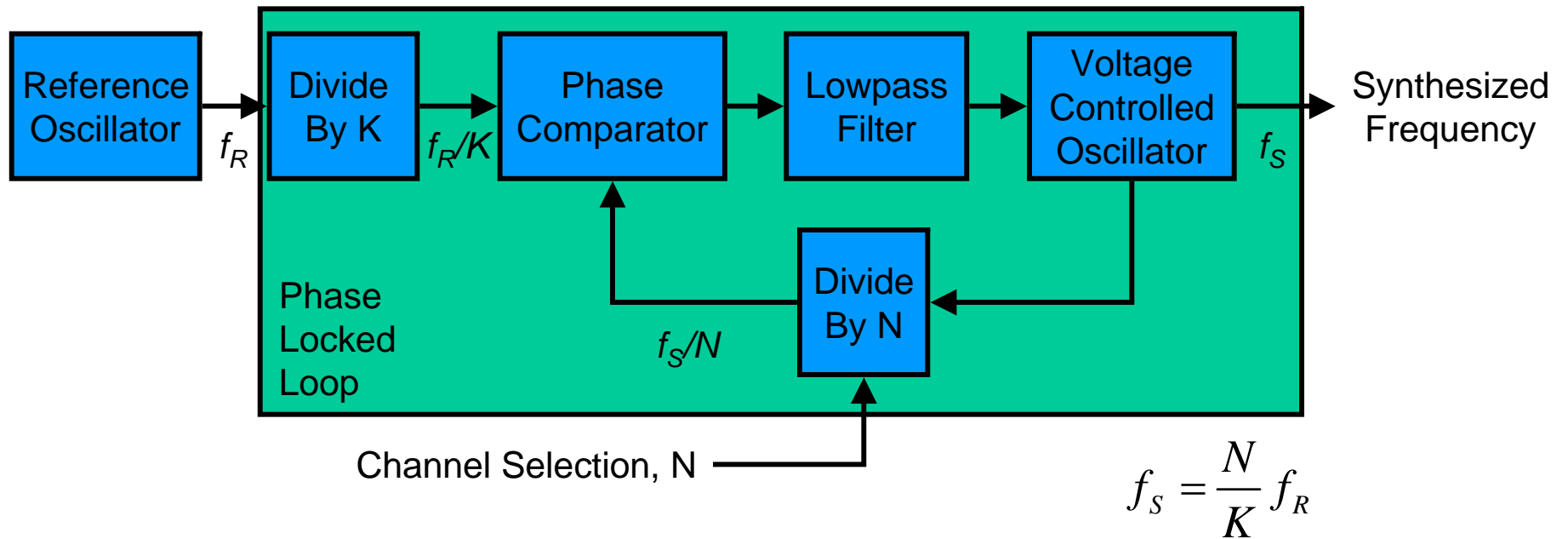
State	Next State	C_{OA}	C_{OB}	C_{OC}
$b_{11}b_{10}b_9b_8 \ b_7b_6b_5b_4 \ b_3b_2b_1b_0$	$b_{11}b_{10}b_9b_8 \ b_7b_6b_5b_4 \ b_3b_2b_1b_0 + 1$	0	0	0
ABCD EFGH 1111	ABCD EFGH+1 0000	1	0	0
ABCD 1111 1111	ABCD+1 0000 0000	1	1	0
1111 1111 1111	$b_{11}b_{10}b_9b_8 \ b_7b_6b_5b_4 \ b_3b_2b_1b_0$	1	1	1

Applications of Programmable Counters

- Programmable divide by N frequency divider:

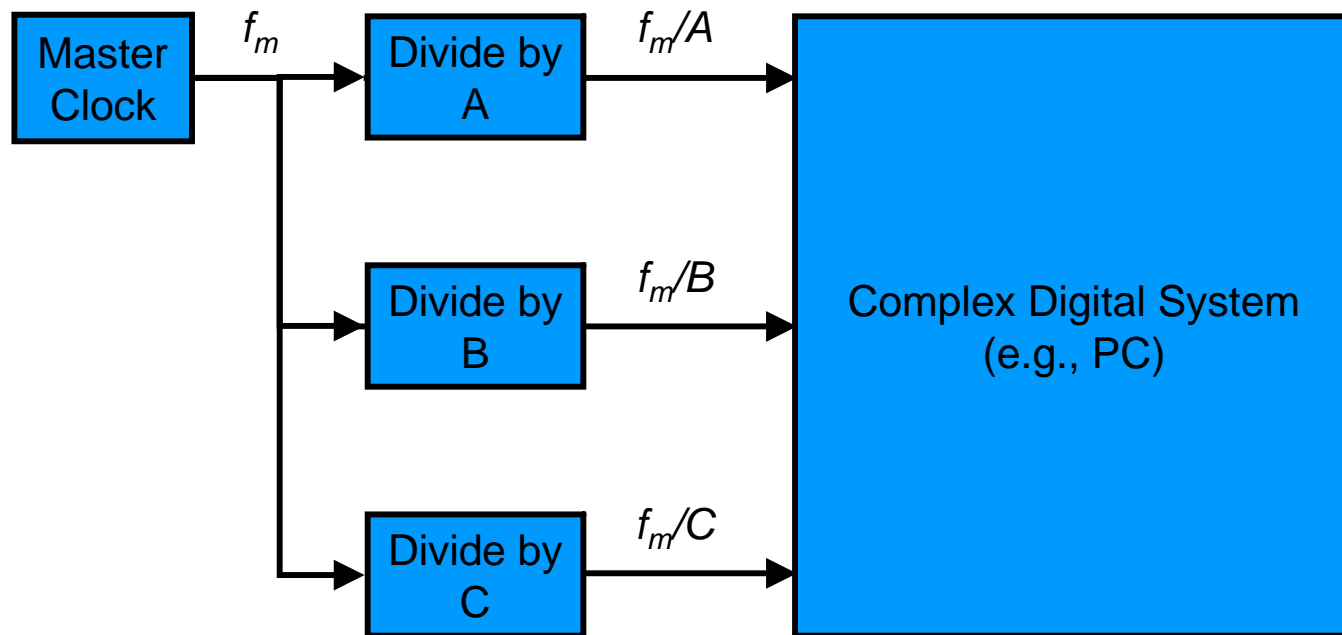


Applications of Programmable Counters

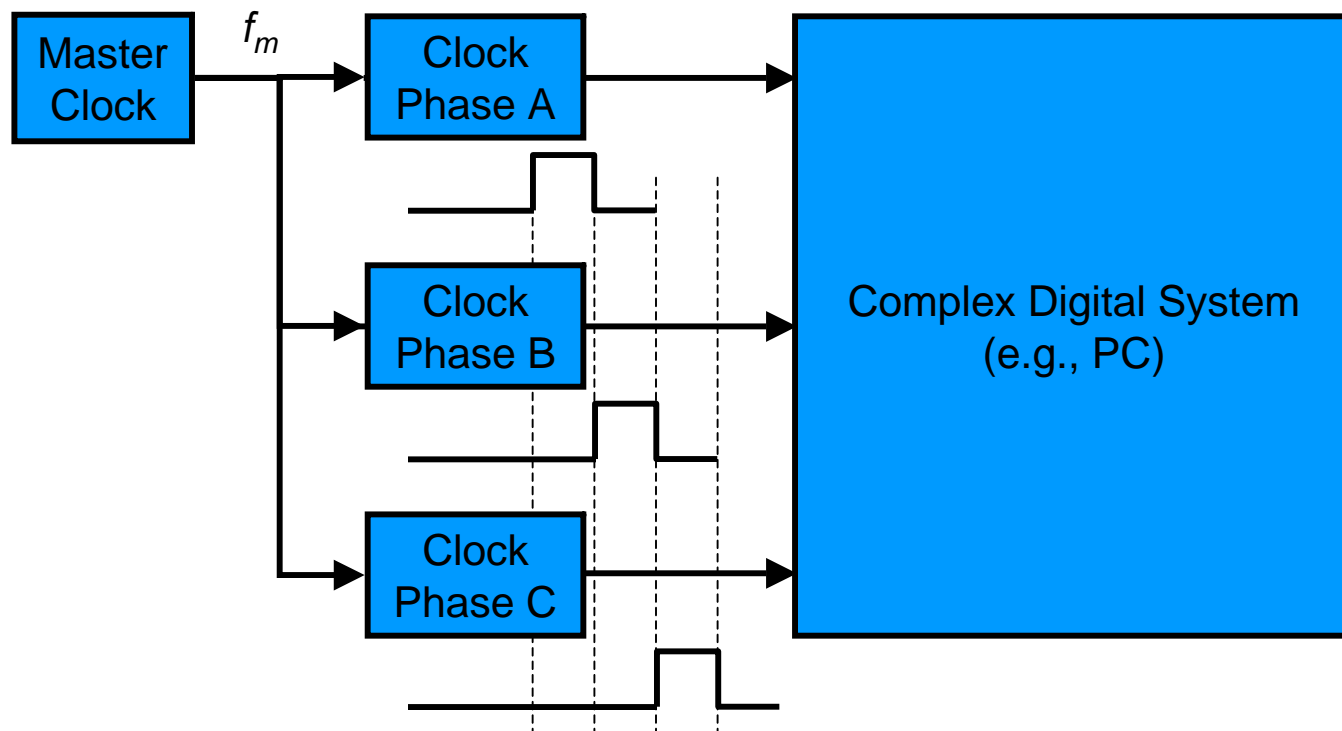


- PLL frequency synthesizers used in
 - TV, radio, cellular phones, PCs, modems, etc.

Applications of Programmable Counters

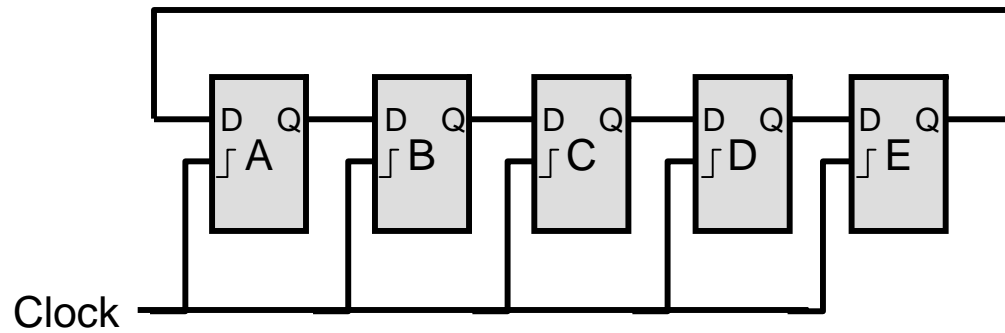


Timing Signal Generation

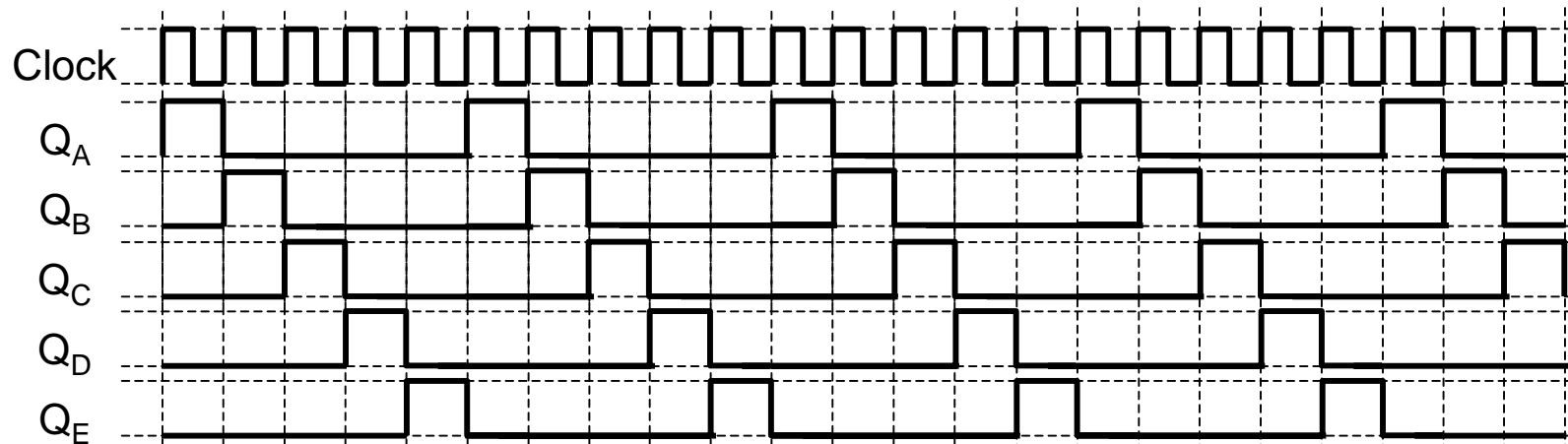


Ring Counters

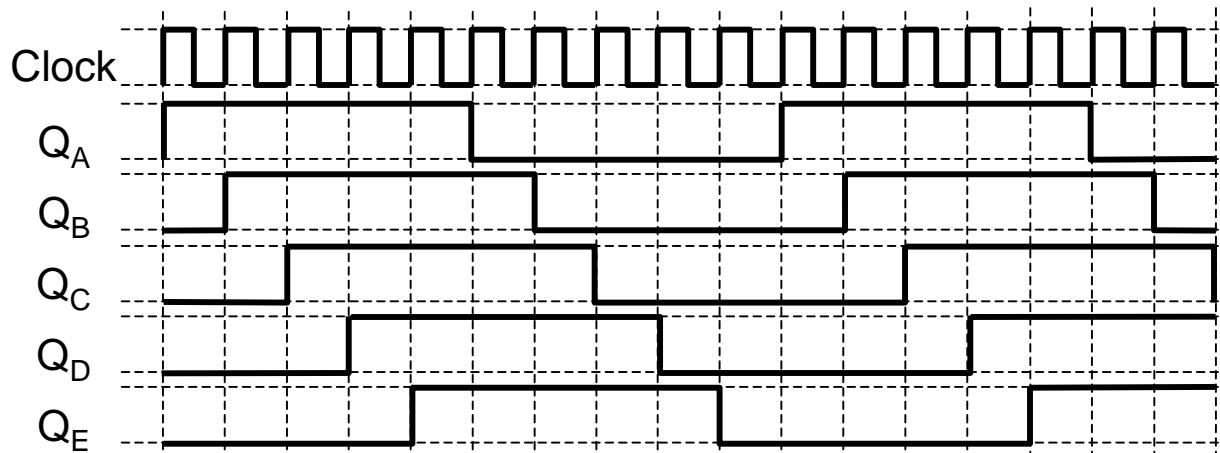
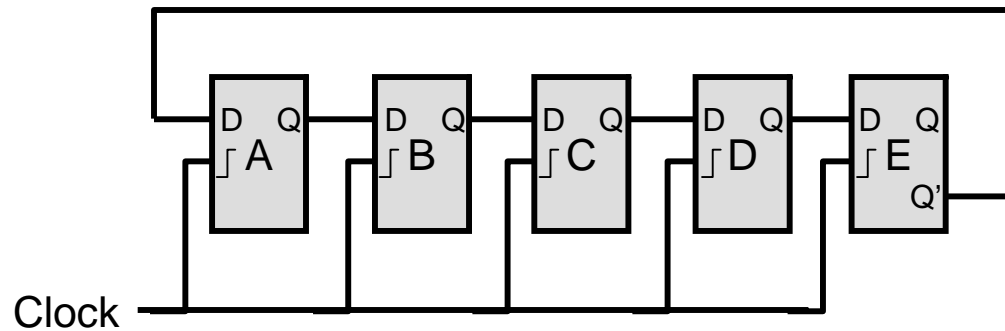
- Only 1 FF is set at any given time



States
10000
01000
00100
00010
00001
10000



“Switch-tail” Ring Counters (Johnson Counter)



States
00000
10000
11000
11100
11110
11111
01111
00111
00011
00001
00000

Summary

- Fundamental concepts of digital systems (Mano Chapter 1)
- Binary codes, number systems, and arithmetic (Ch 1)
- Boolean algebra (Ch 2)
- Simplification of switching equations (Ch 3)
- Digital device characteristics (e.g., TTL, CMOS)/design considerations (Ch 10)
- Combinatoric logical design including LSI implementation (Chapter 4)
- Flip-flops and state memory elements (Ch 5)
- Sequential logic analysis and design (Ch 5)
- **Counters, shift register circuits (Ch 6)**
- Hazards, Races, and time related issues in digital design (Ch 9)
- Synchronous vs. asynchronous design (Ch 9)
- Memory and Programmable logic (Ch 7)
- Minimization of sequential systems
- Introduction to Finite Automata

Homework 10 – due in Class 12

- Show all work
- Problems 6-11, 6-23, 6-29