

Real-Time Embedded Systems

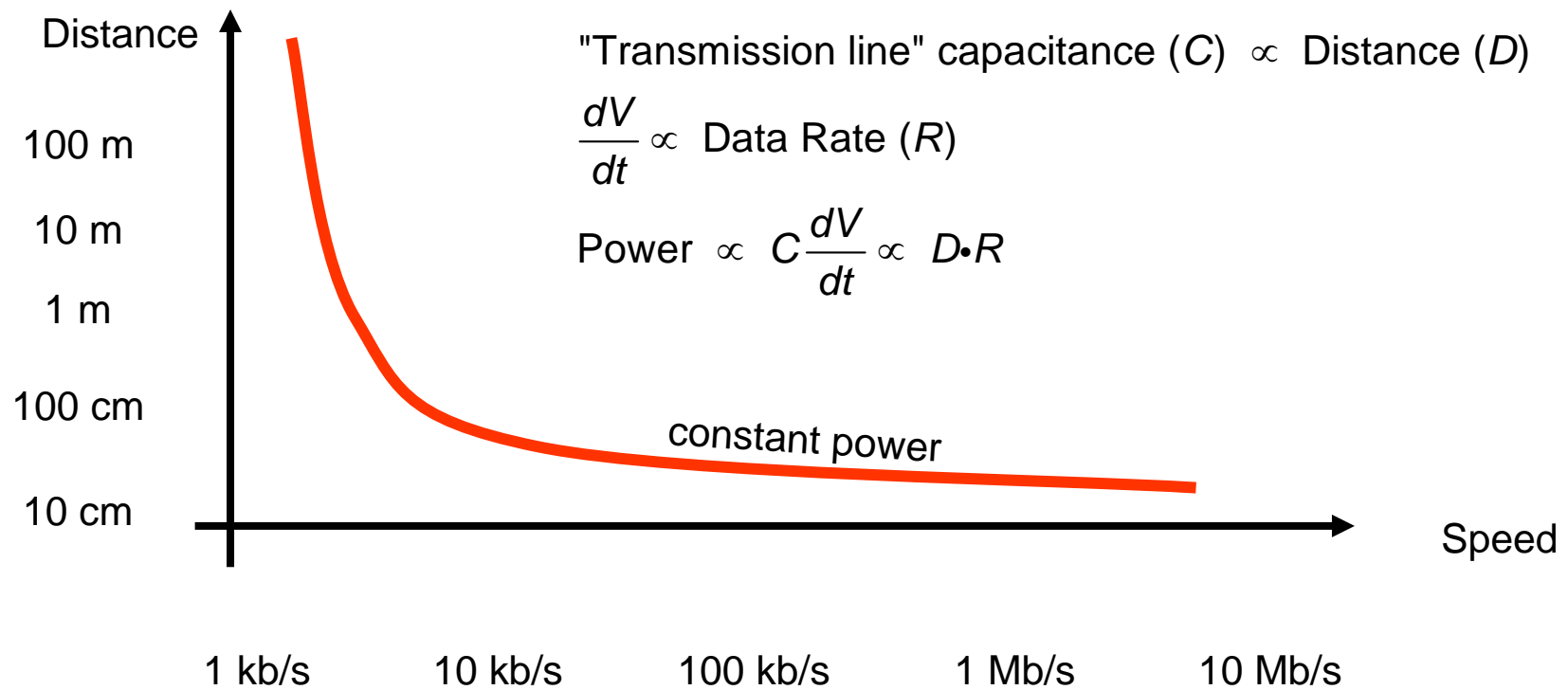
CpE-450 Spring 06

Class 5

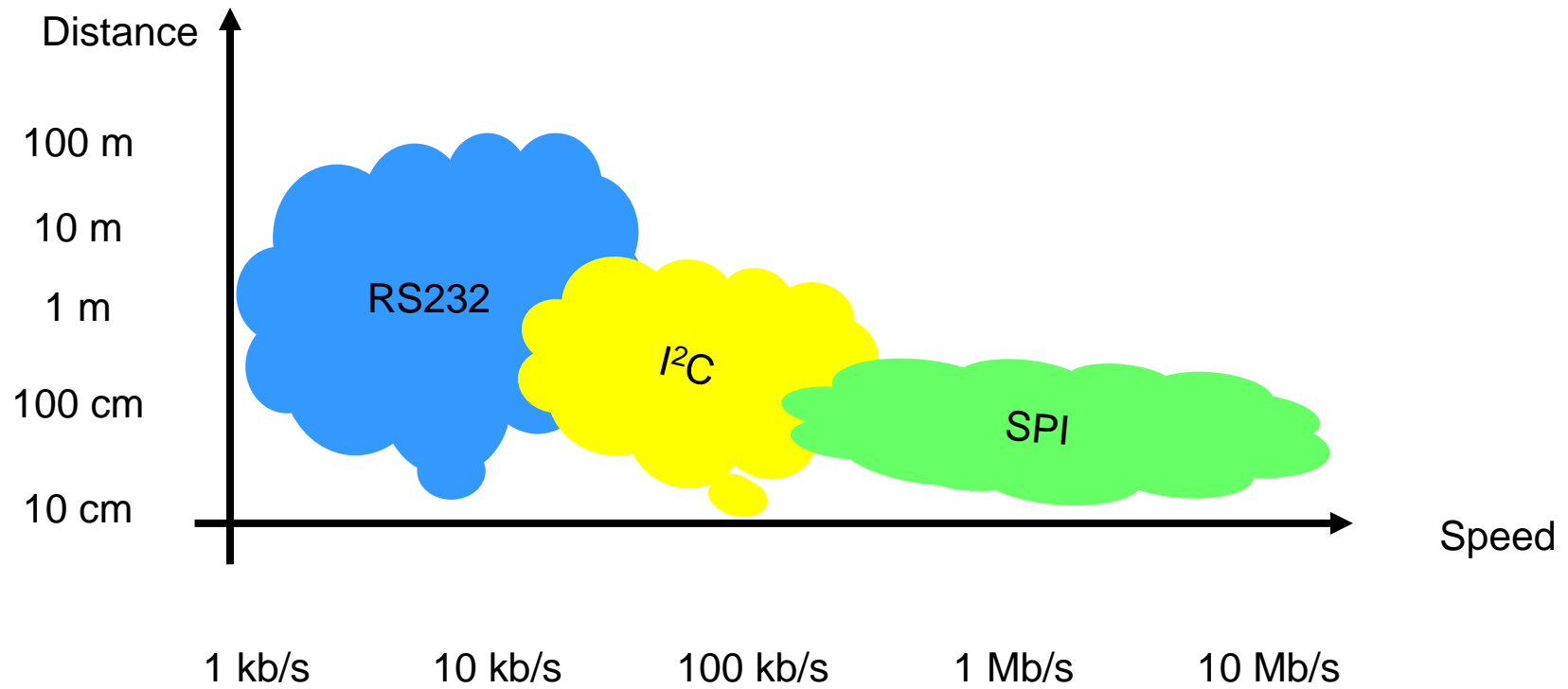
Bruce McNair

bmcnair@stevens.edu

Interfacing to Embedded Systems

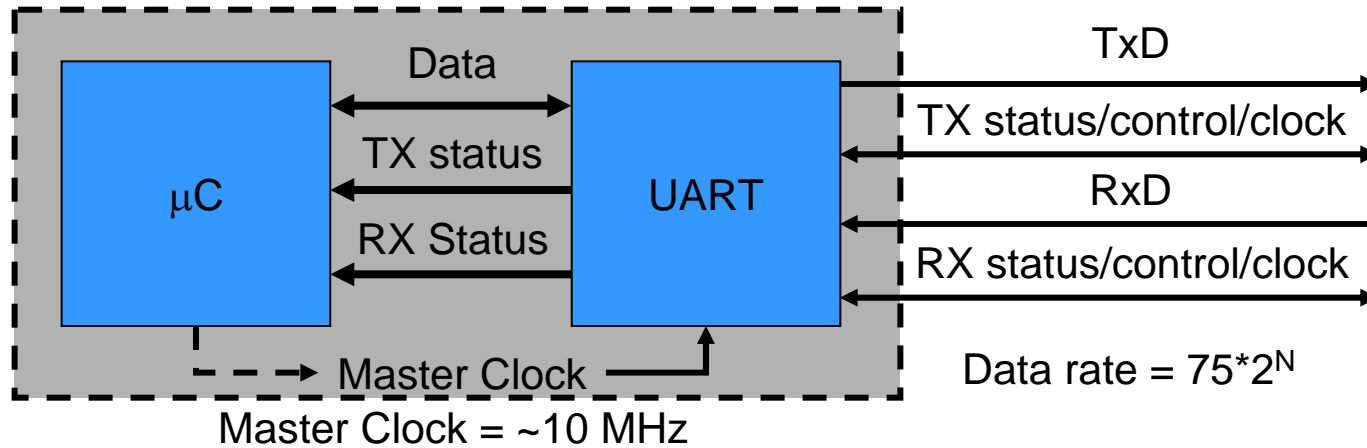


Interfacing to Embedded Systems



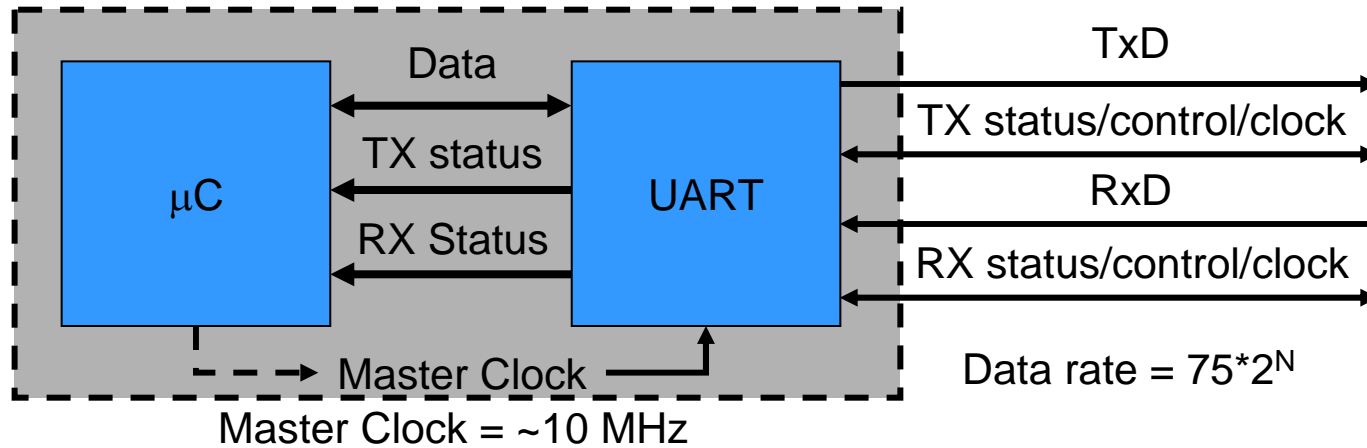
Embedded System Interfacing

- RS-232 Serial Communications



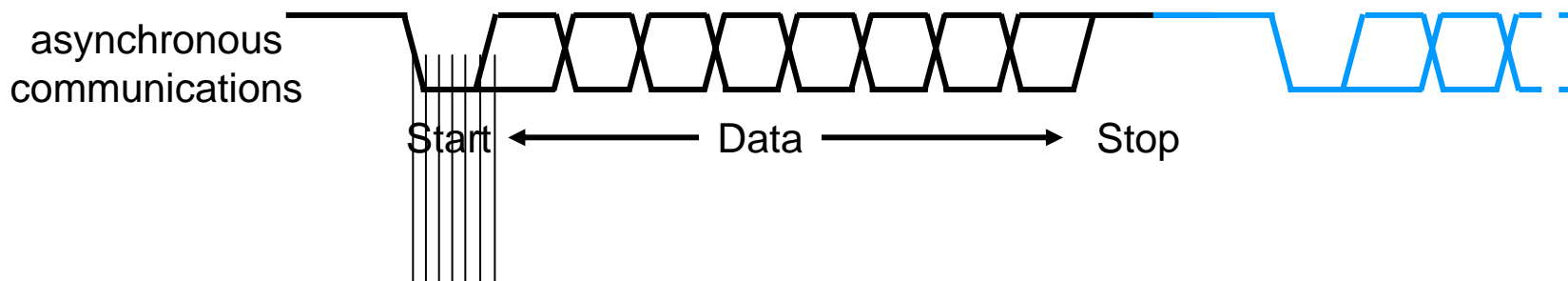
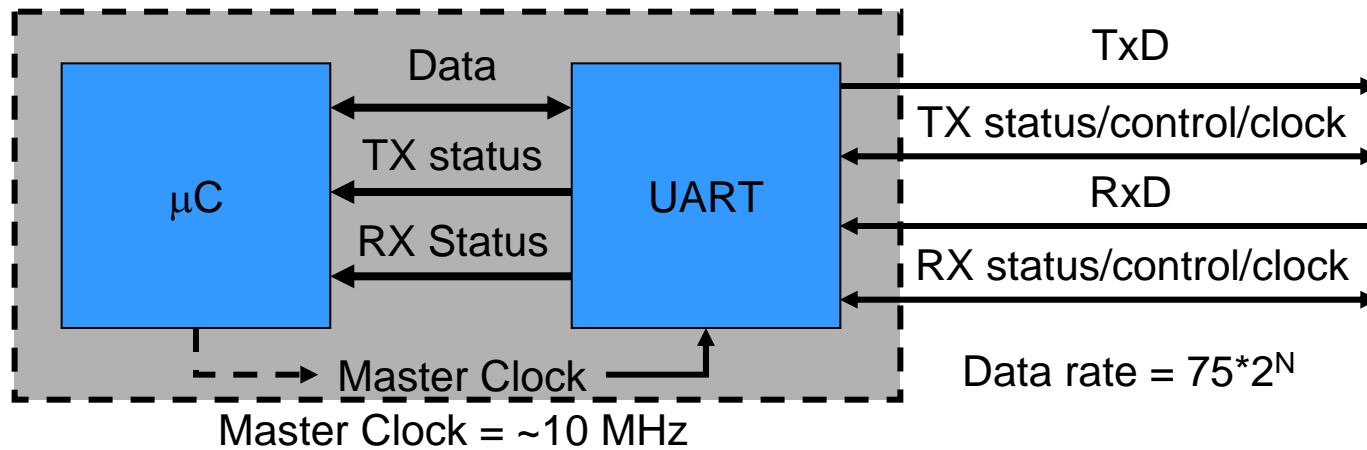
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- RS-232 Serial Communications



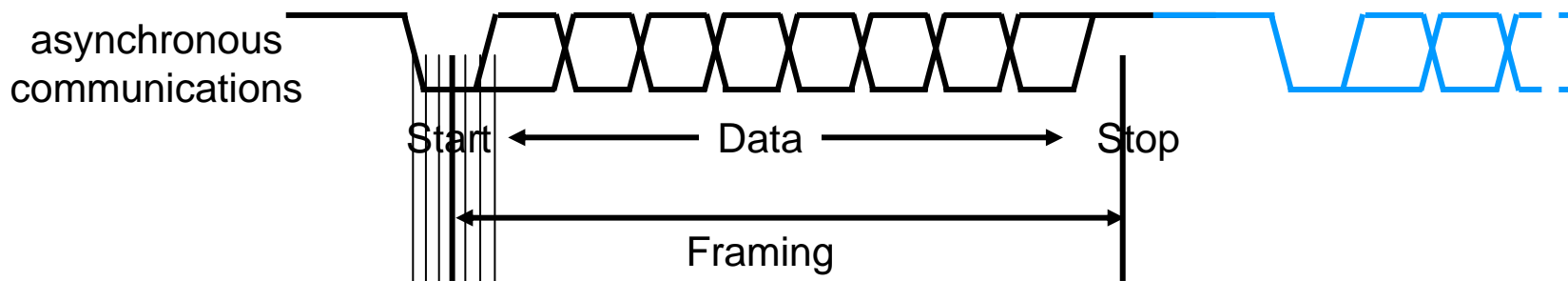
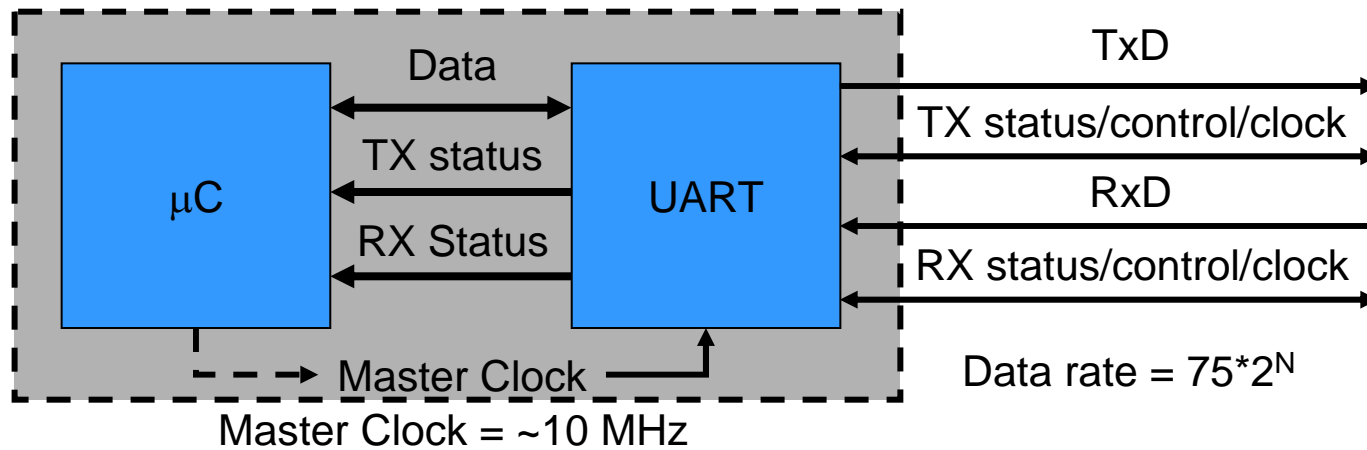
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- RS-232 Serial Communications



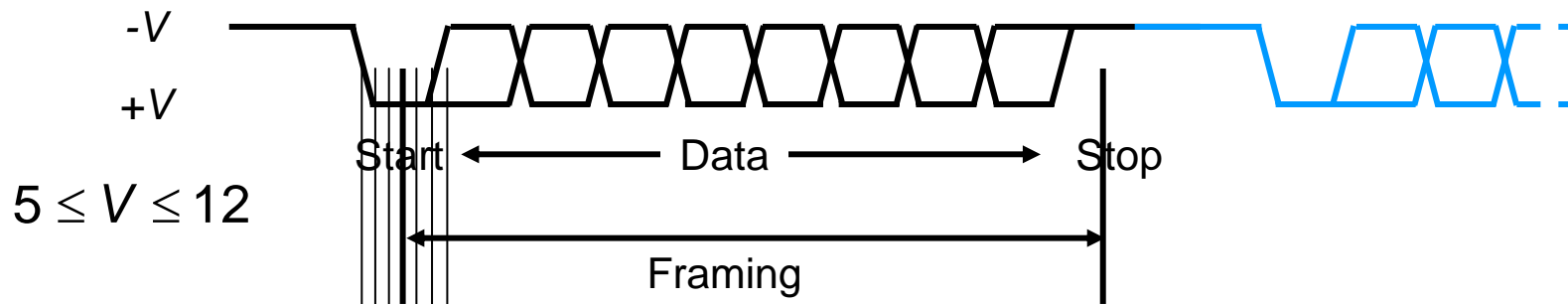
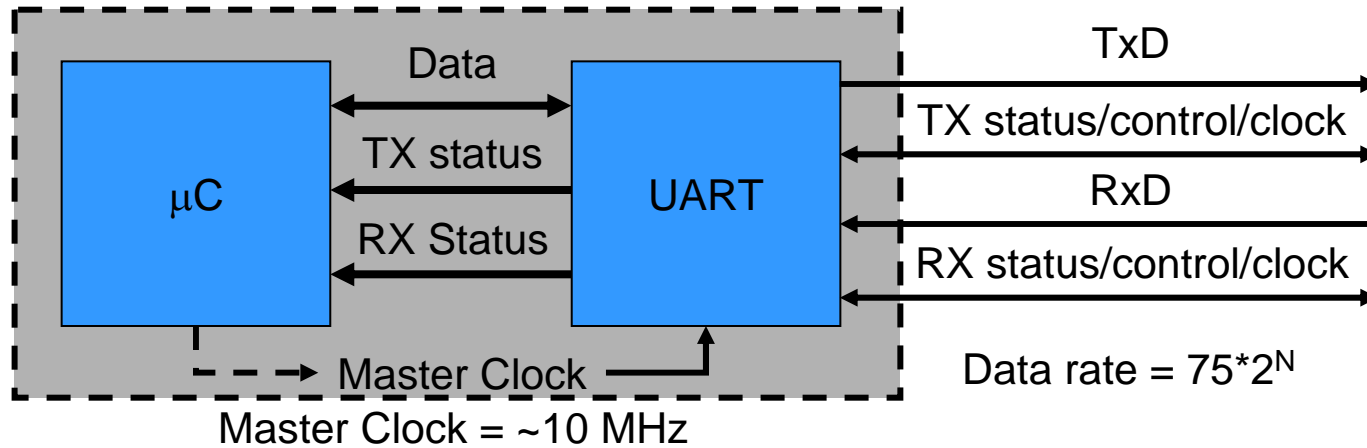
Embedded System Interfacing

- RS-232 Serial Communications



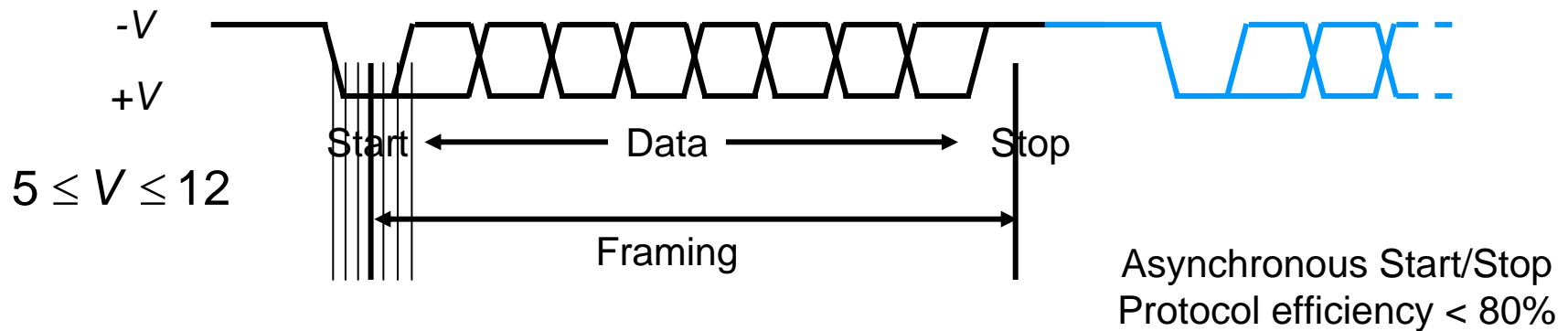
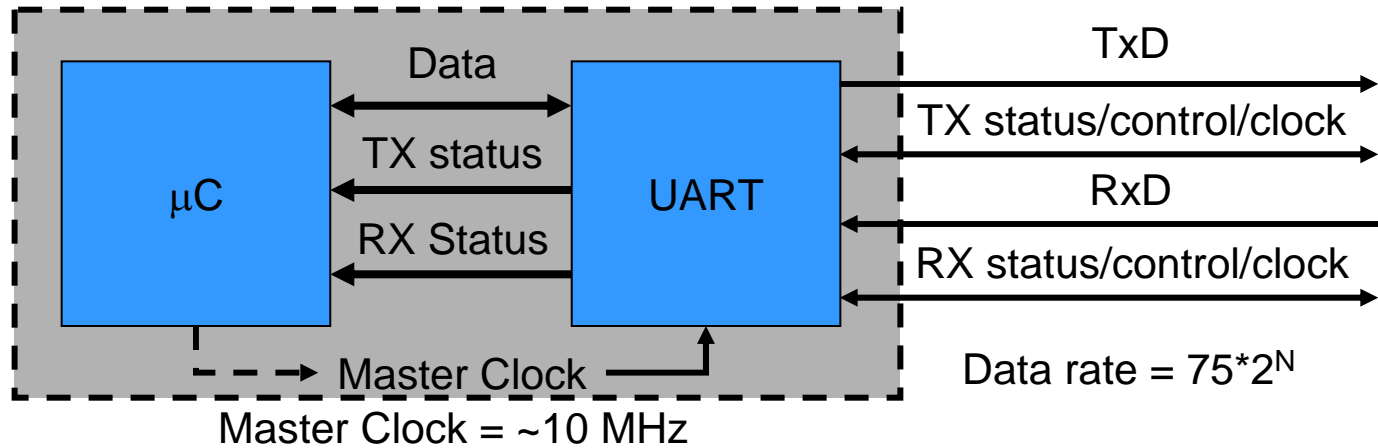
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- RS-232 Serial Communications



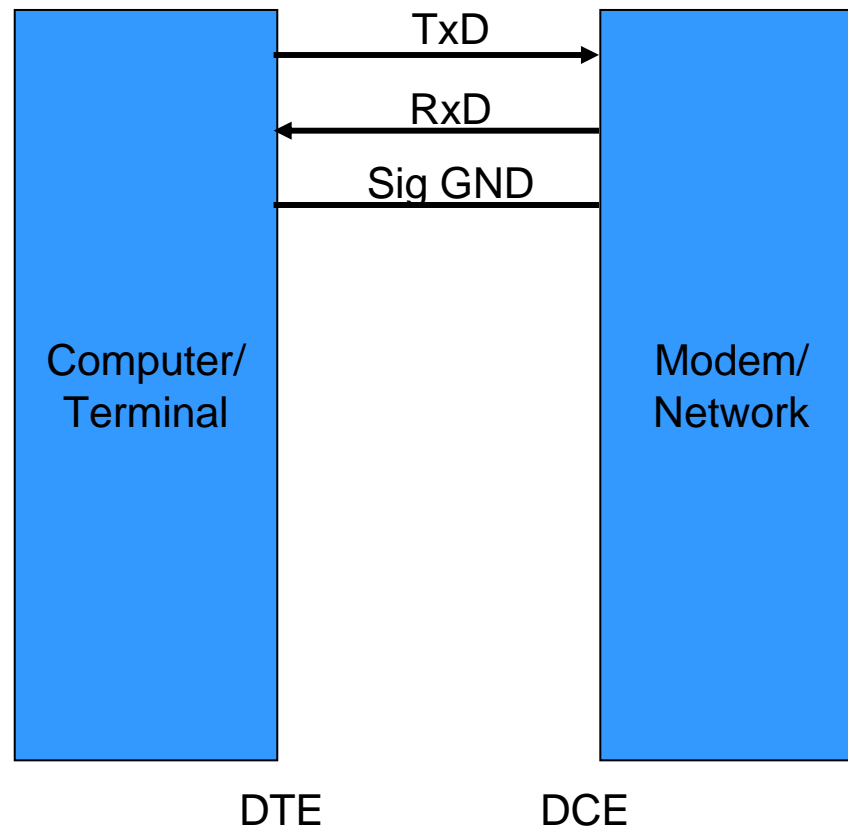
Embedded System Interfacing

- RS-232 Serial Communications



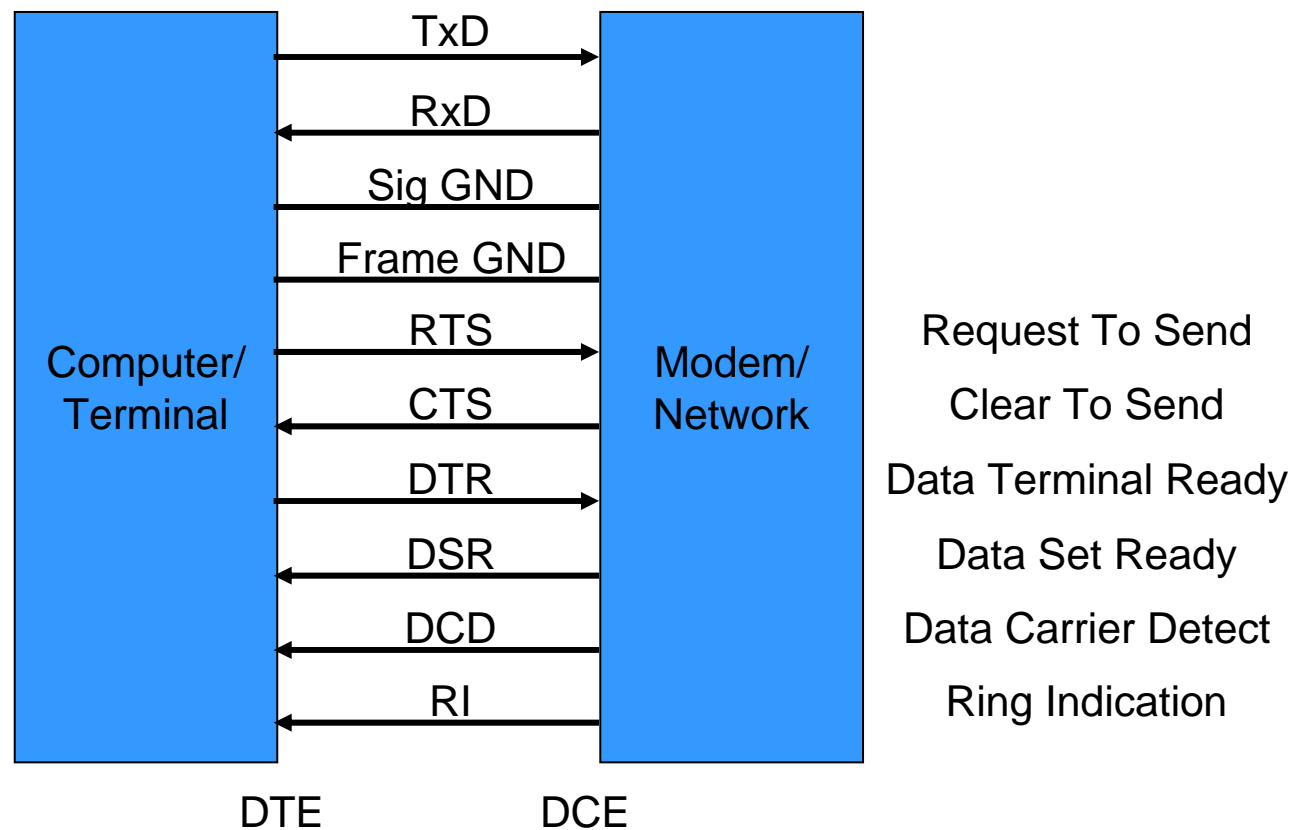
Embedded System Interfacing

- RS-232 Serial Communications



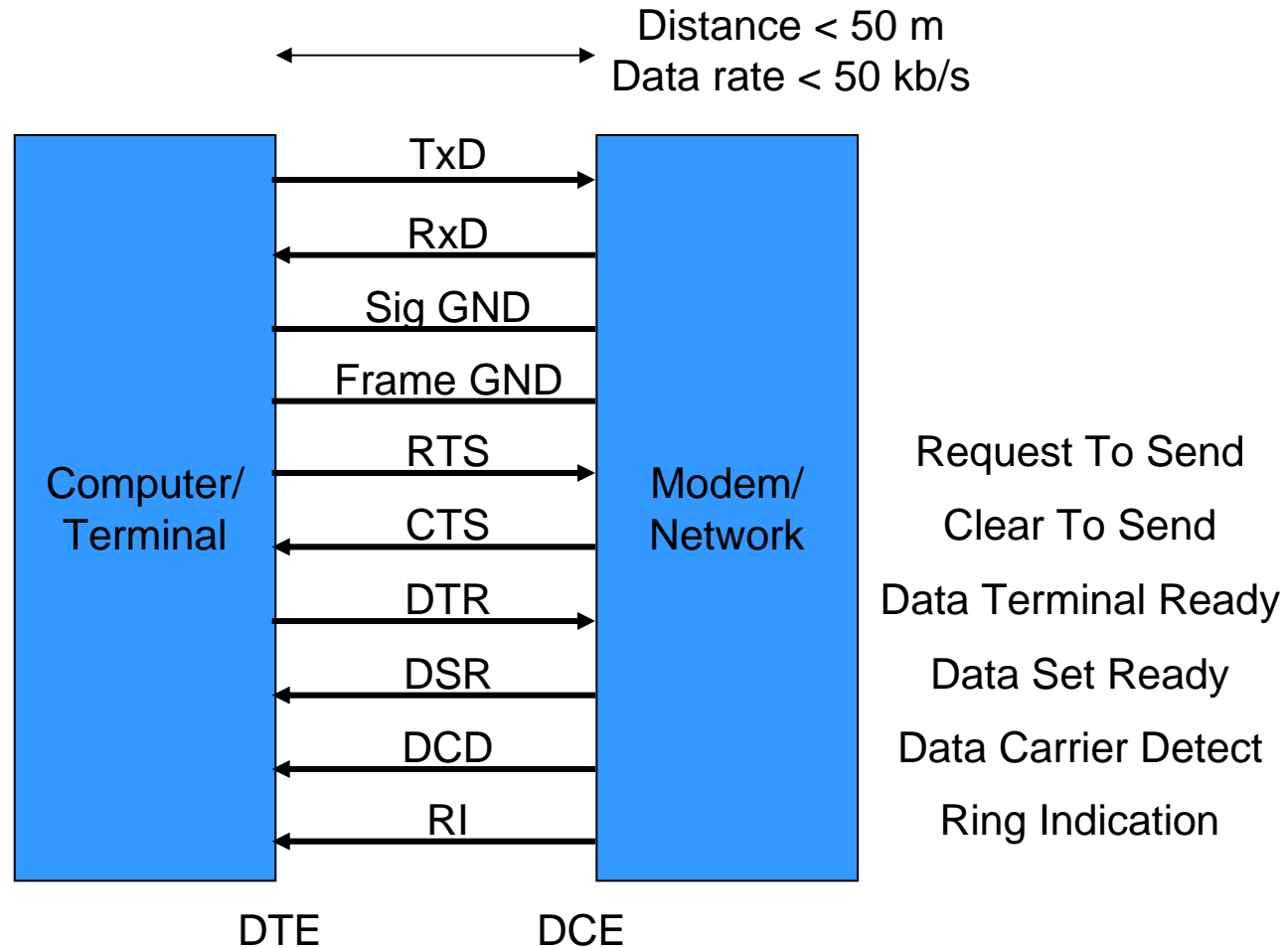
Embedded System Interfacing

- RS-232 Serial Communications



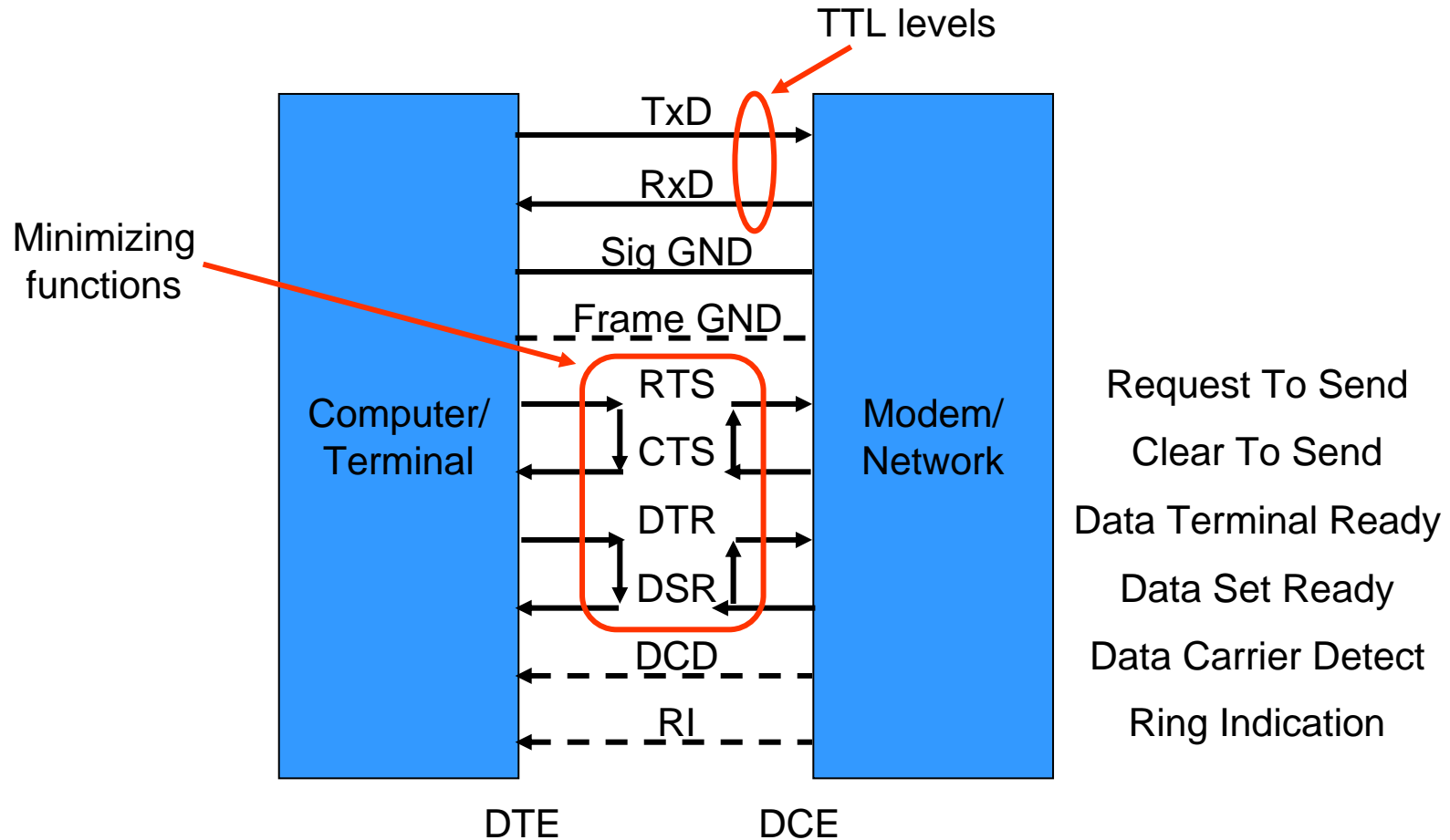
Embedded System Interfacing

- RS-232 Serial Communications



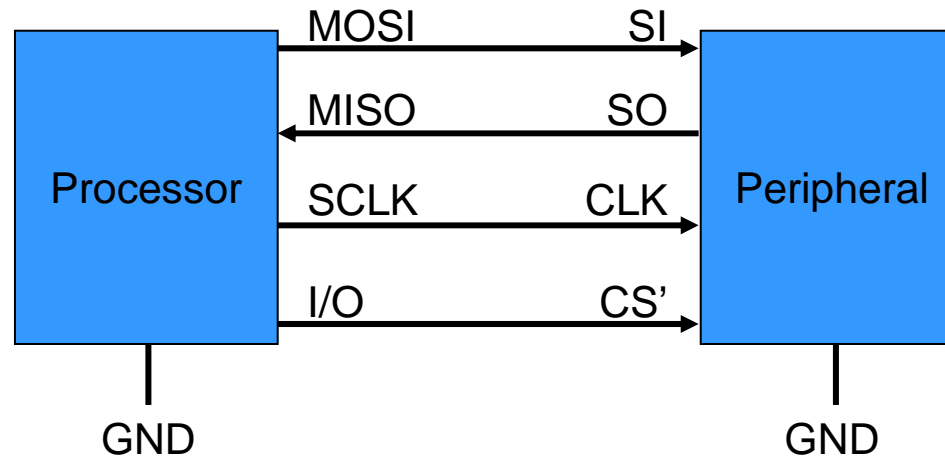
Embedded System Interfacing

- RS-232 Serial Communications - variations



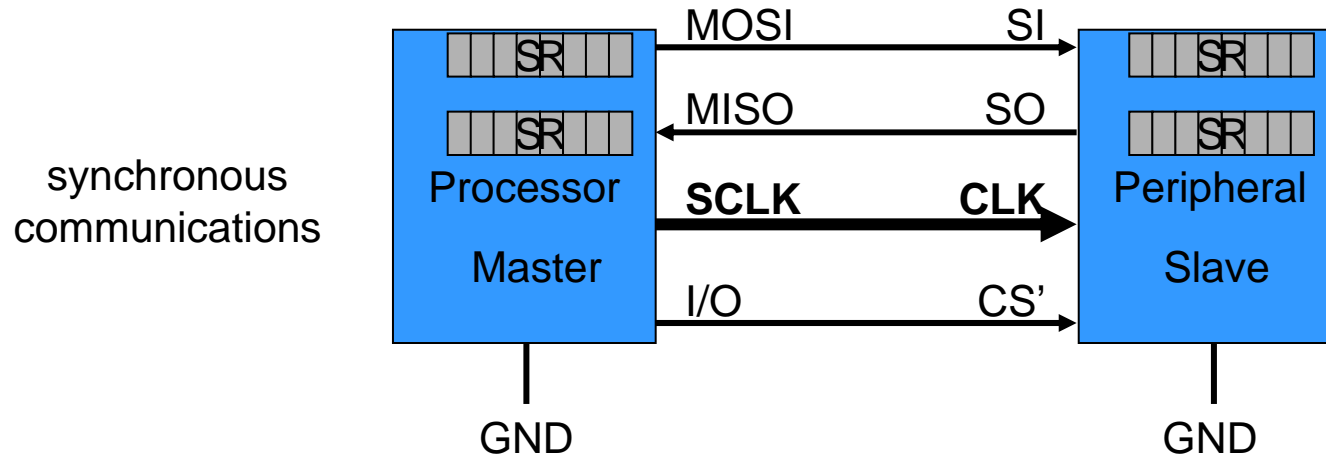
Embedded Systems Interfacing

- SPI – Serial Peripheral Interface



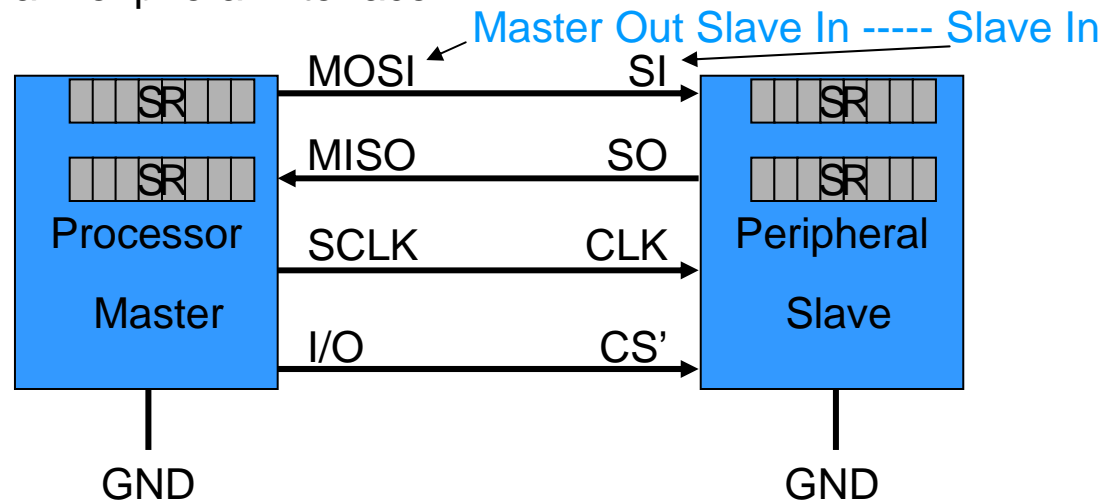
Embedded Systems Interfacing

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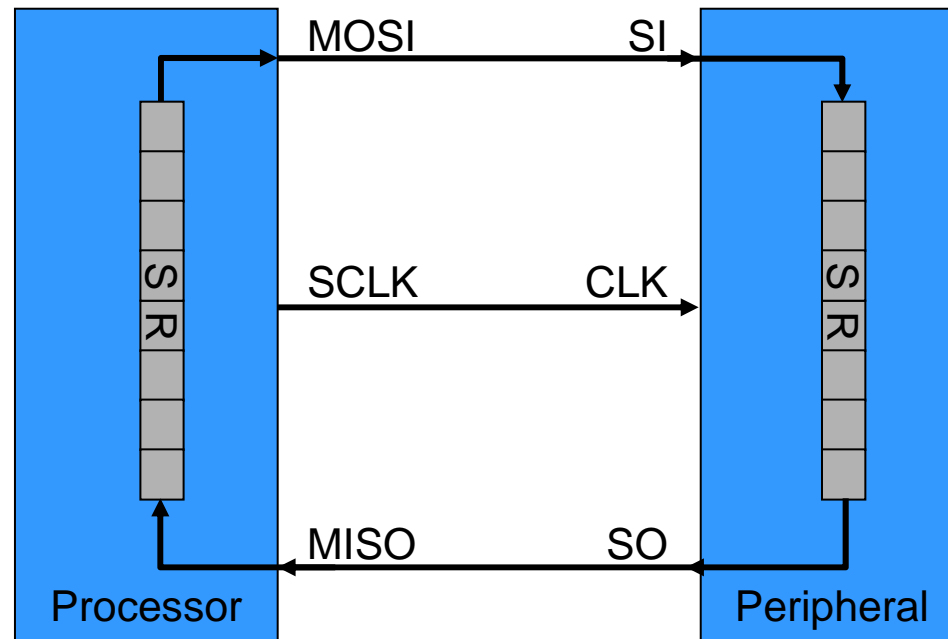
Embedded Systems Interfacing

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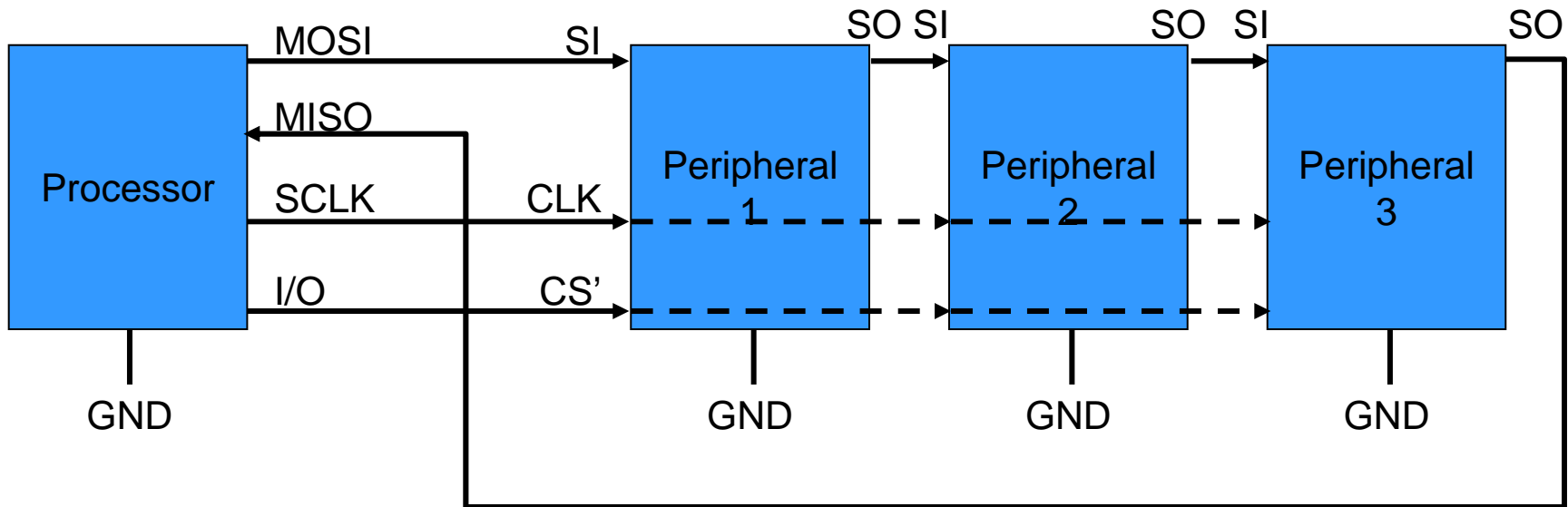
Embedded Systems Interfacing

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Embedded Systems Interfacing

- SPI – Serial Peripheral Interface



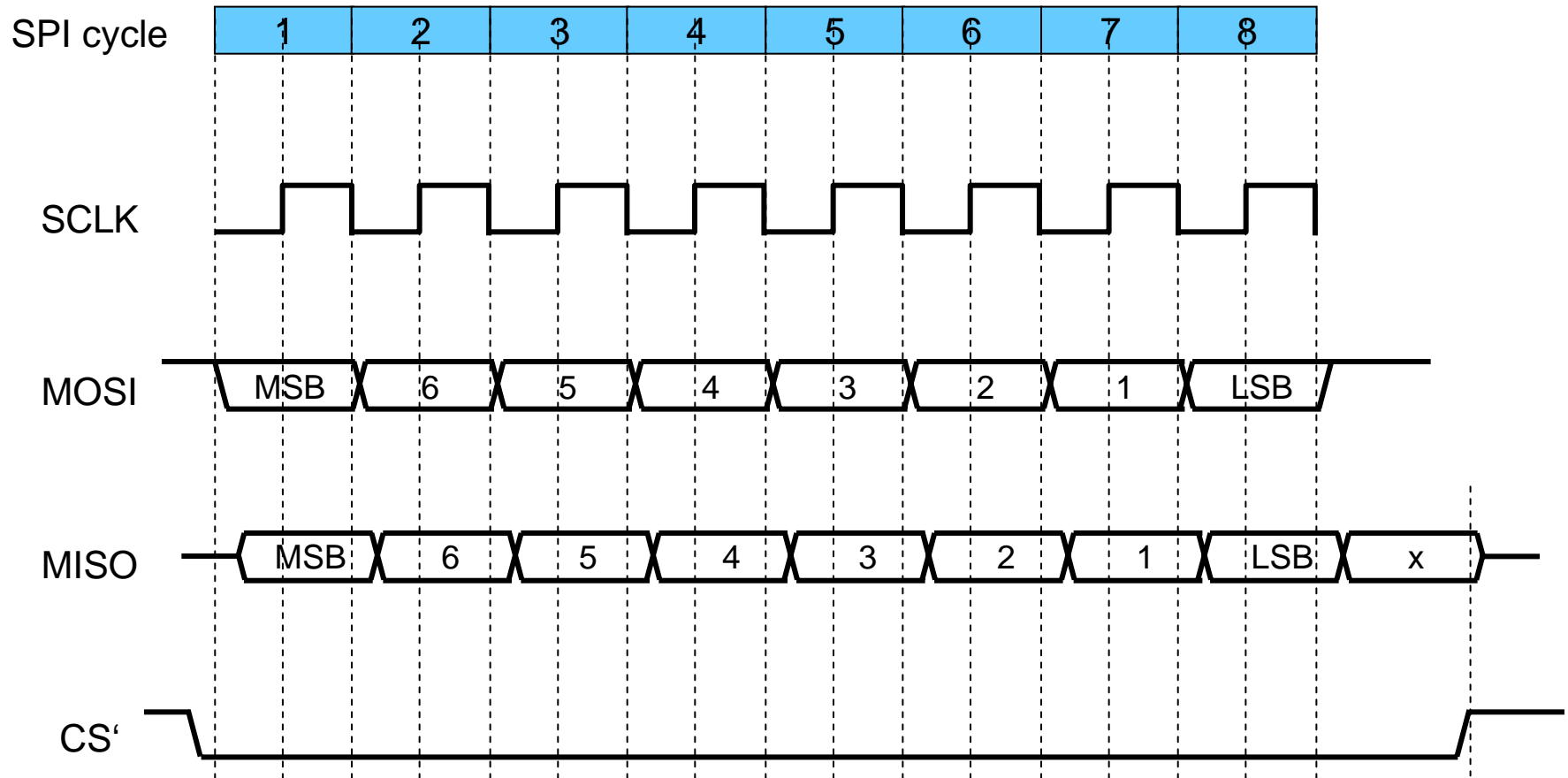
Extension to multiple peripherals:

- Real Time Clocks (time of day)
- Sensors (e.g. potentiometers)
- FLASH memory

- Interface speed limited by device technology Mb/s, compared to kb/s for RS-232

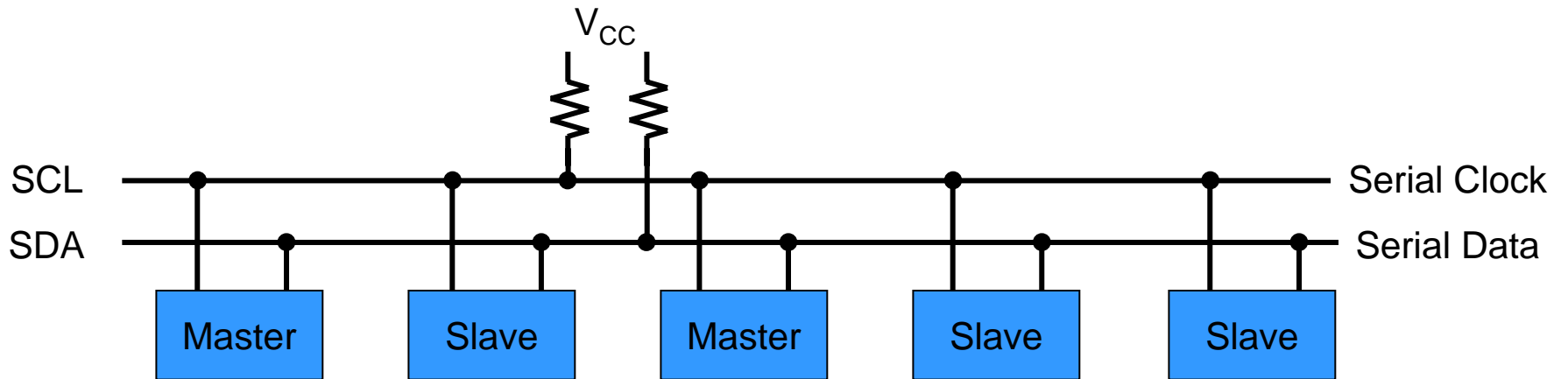
Embedded Systems Interfacing

- SPI timing (Clock low, Clock phase 0)



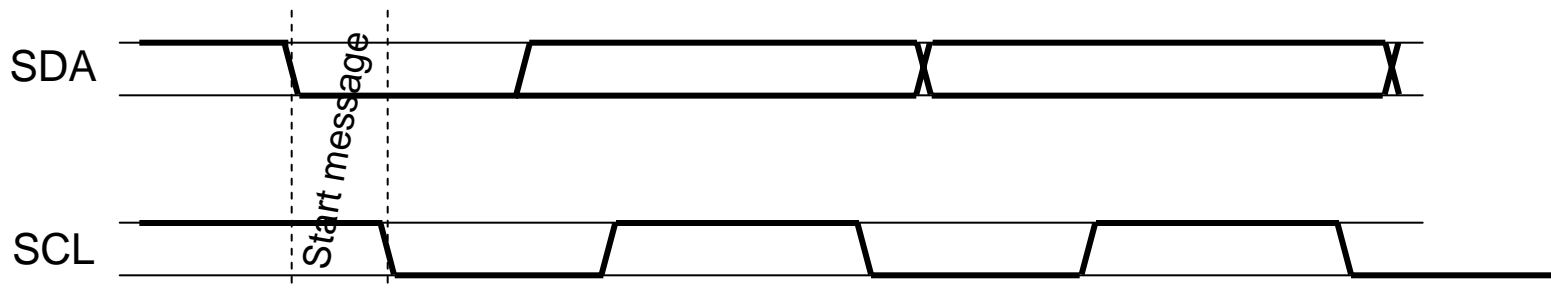
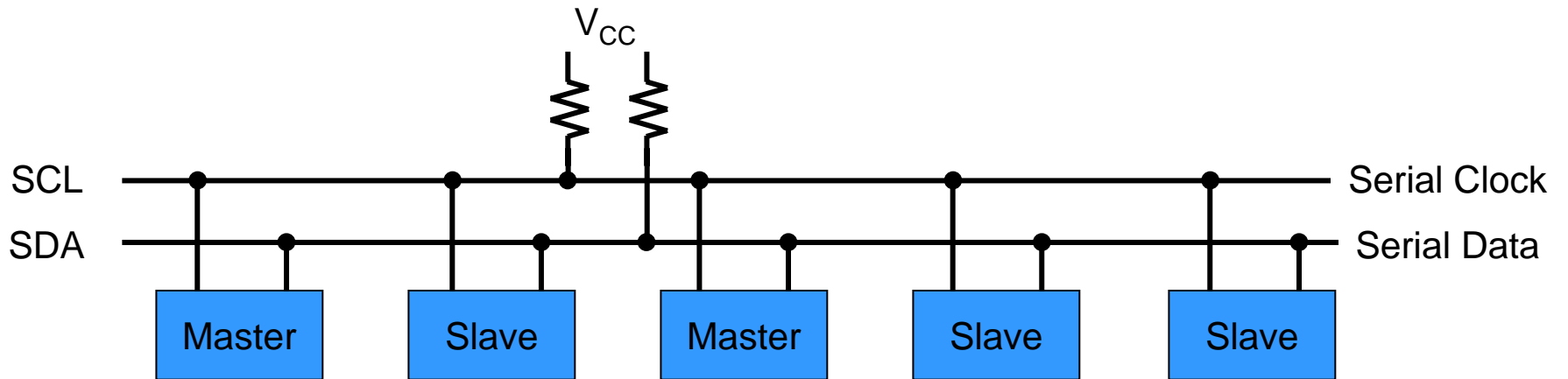
Embedded Systems Interfacing

- I²C – Inter Integrated Circuit



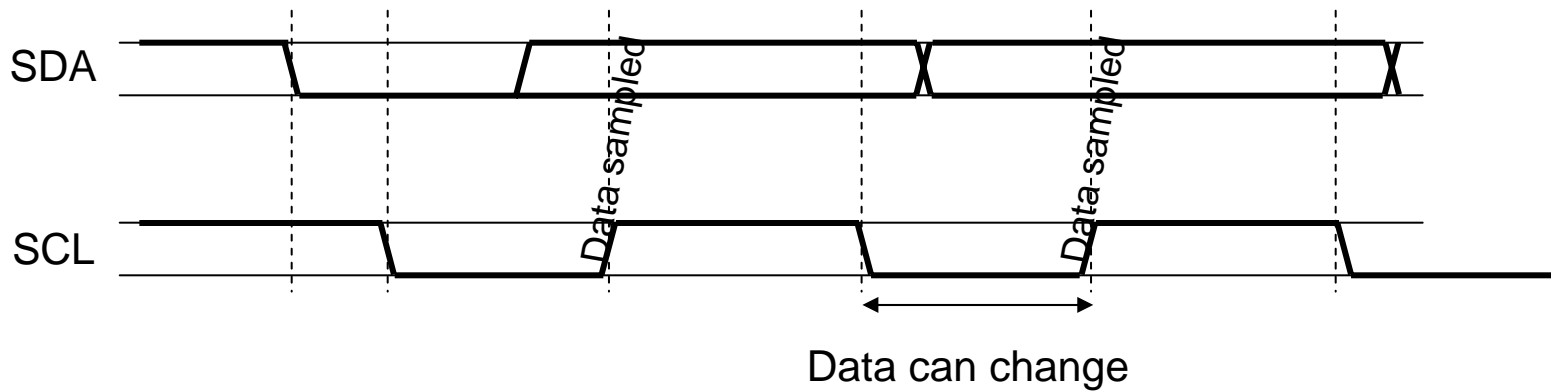
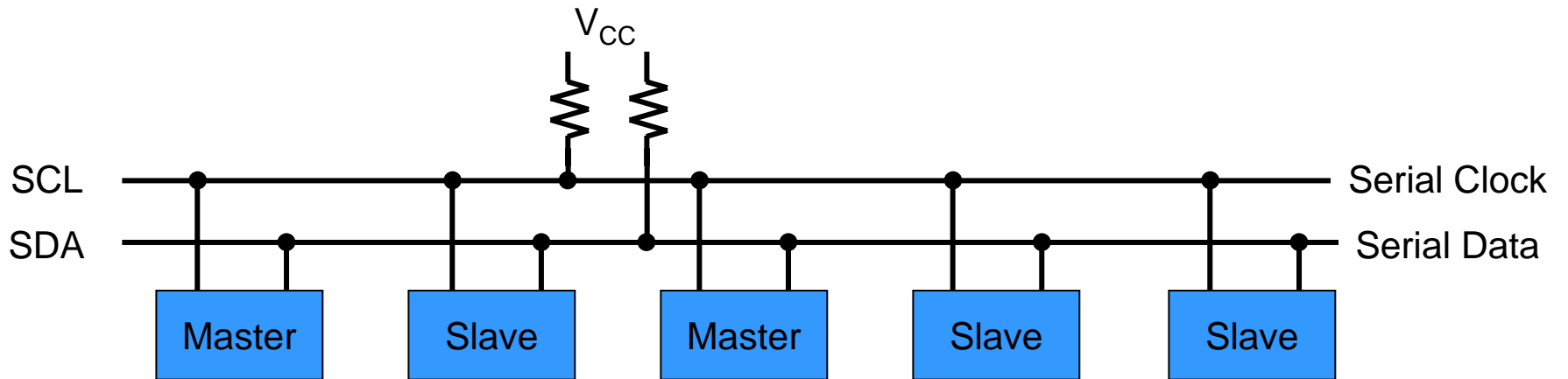
Embedded Systems Interfacing

- I²C – Inter Integrated Circuit



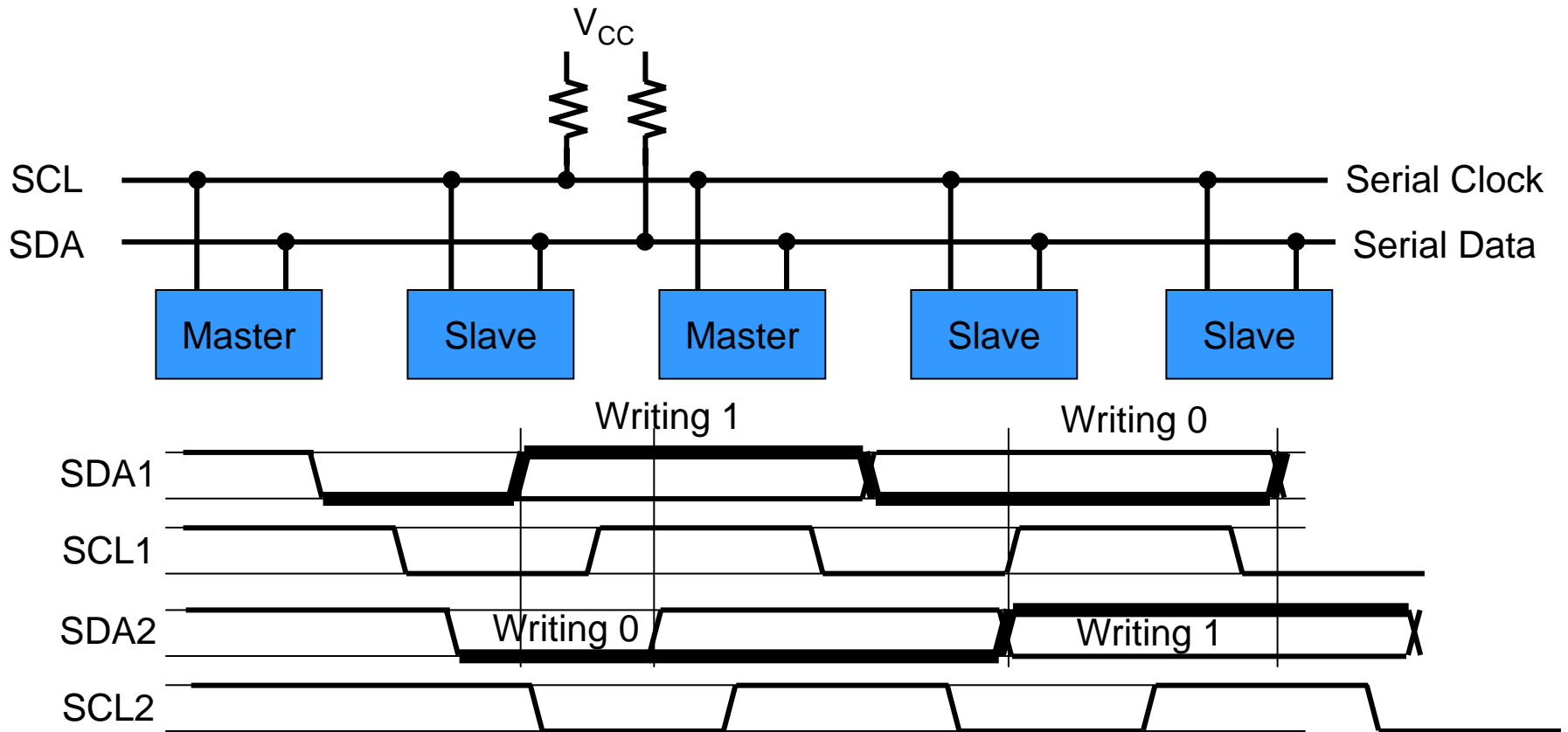
Embedded Systems Interfacing

- I²C – Inter Integrated Circuit



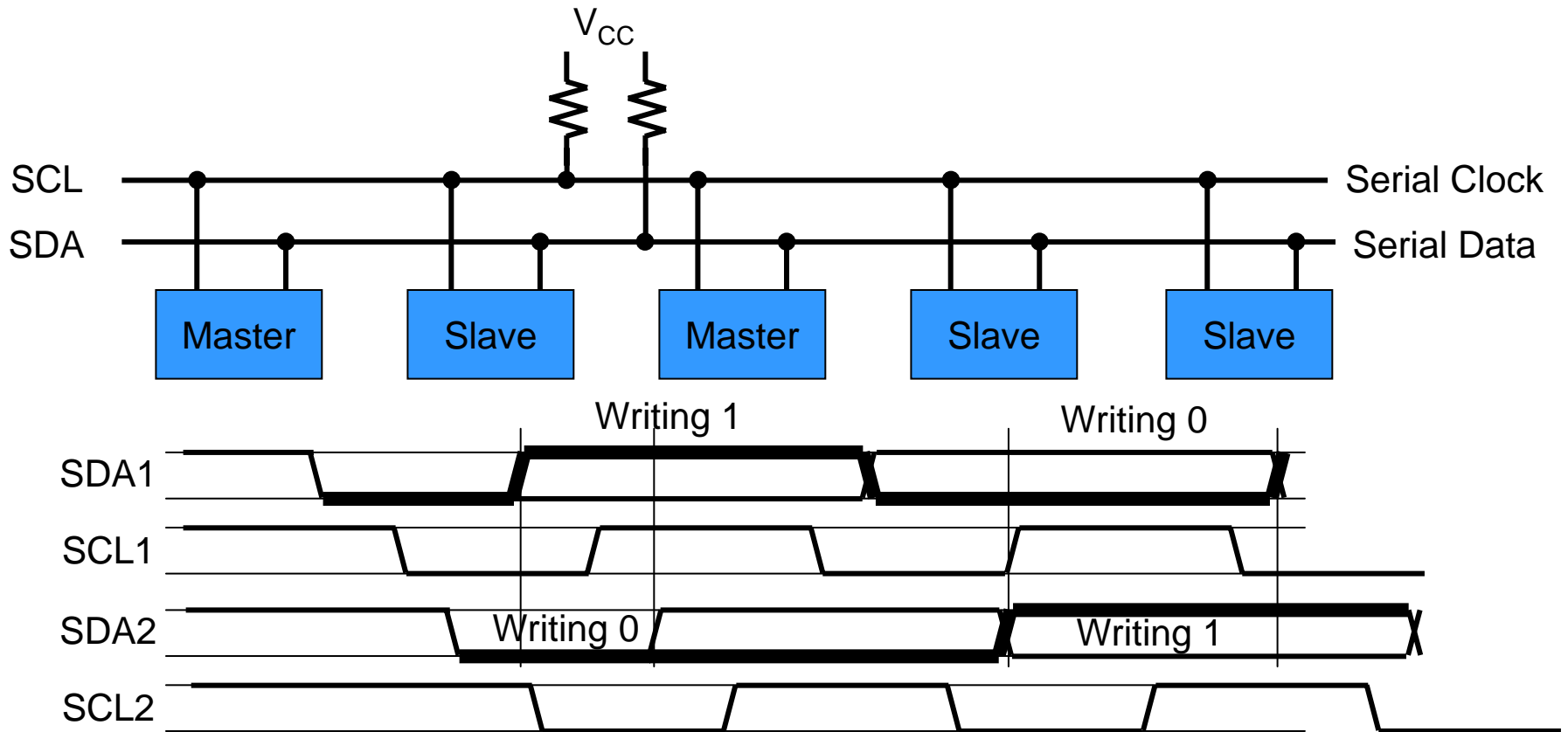
Embedded Systems Interfacing

- I²C – Inter Integrated Circuit – Multi-master bus



Embedded Systems Interfacing

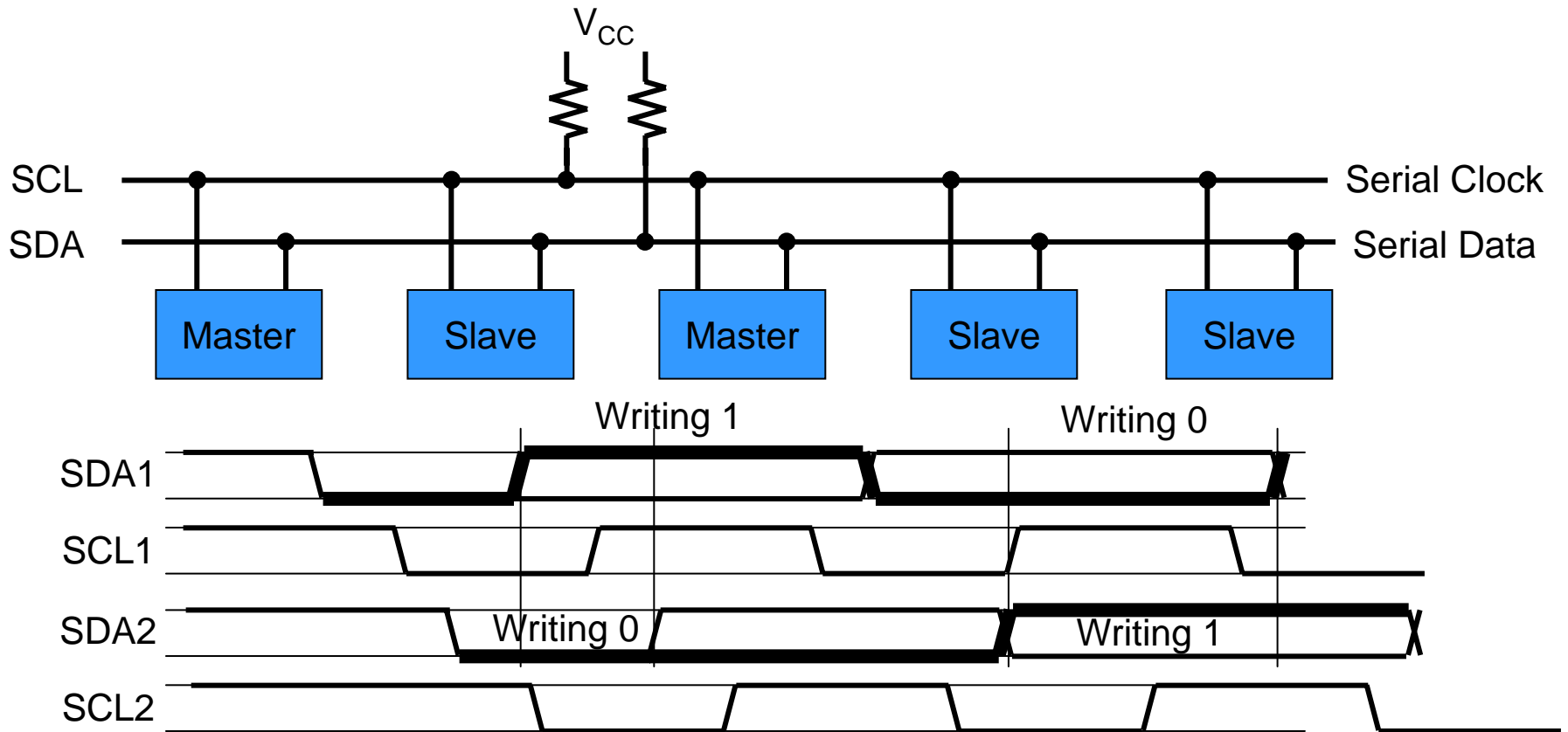
- I²C – Inter Integrated Circuit – Multi-master bus



- Device writing “1” passively allows pullup resistors to pull bus to “1”
- Device writing “0” actively sets bus to “0”

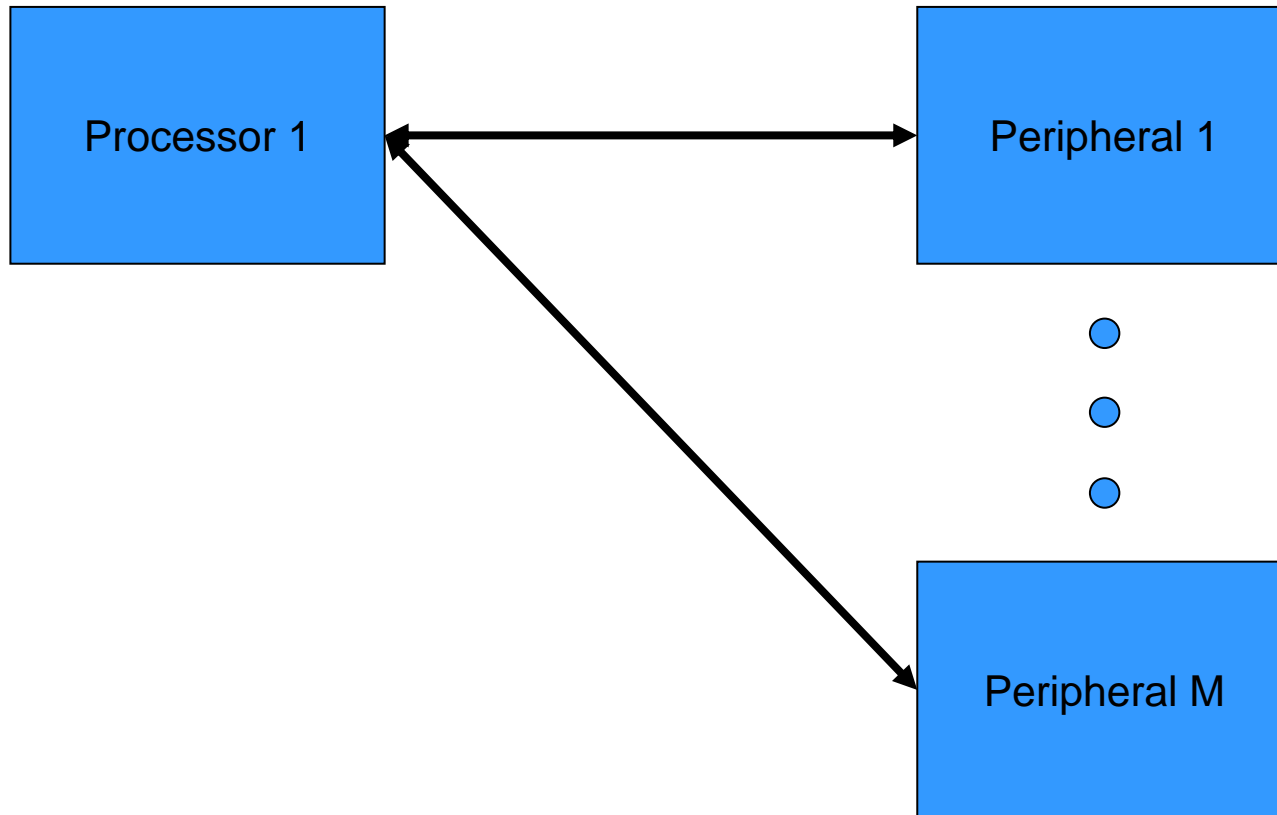
Embedded Systems Interfacing

- I²C – Inter Integrated Circuit – Multi-master bus

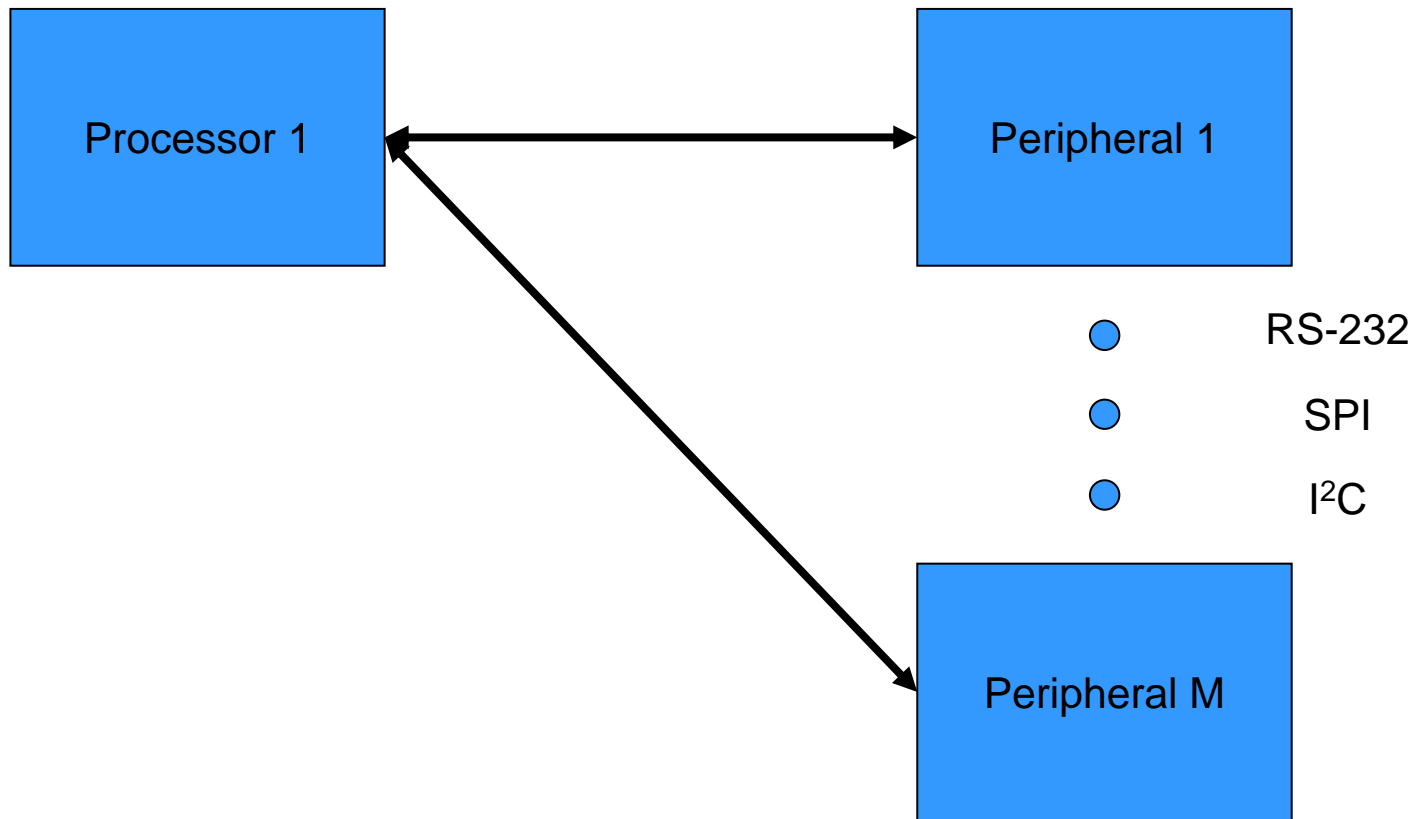


- Device writing “1” passively allows pullup resistors to pull bus to “1”
- Device writing “0” actively sets bus to “0”
- Device that writes “1” but hears “0” aborts transmission and tries later

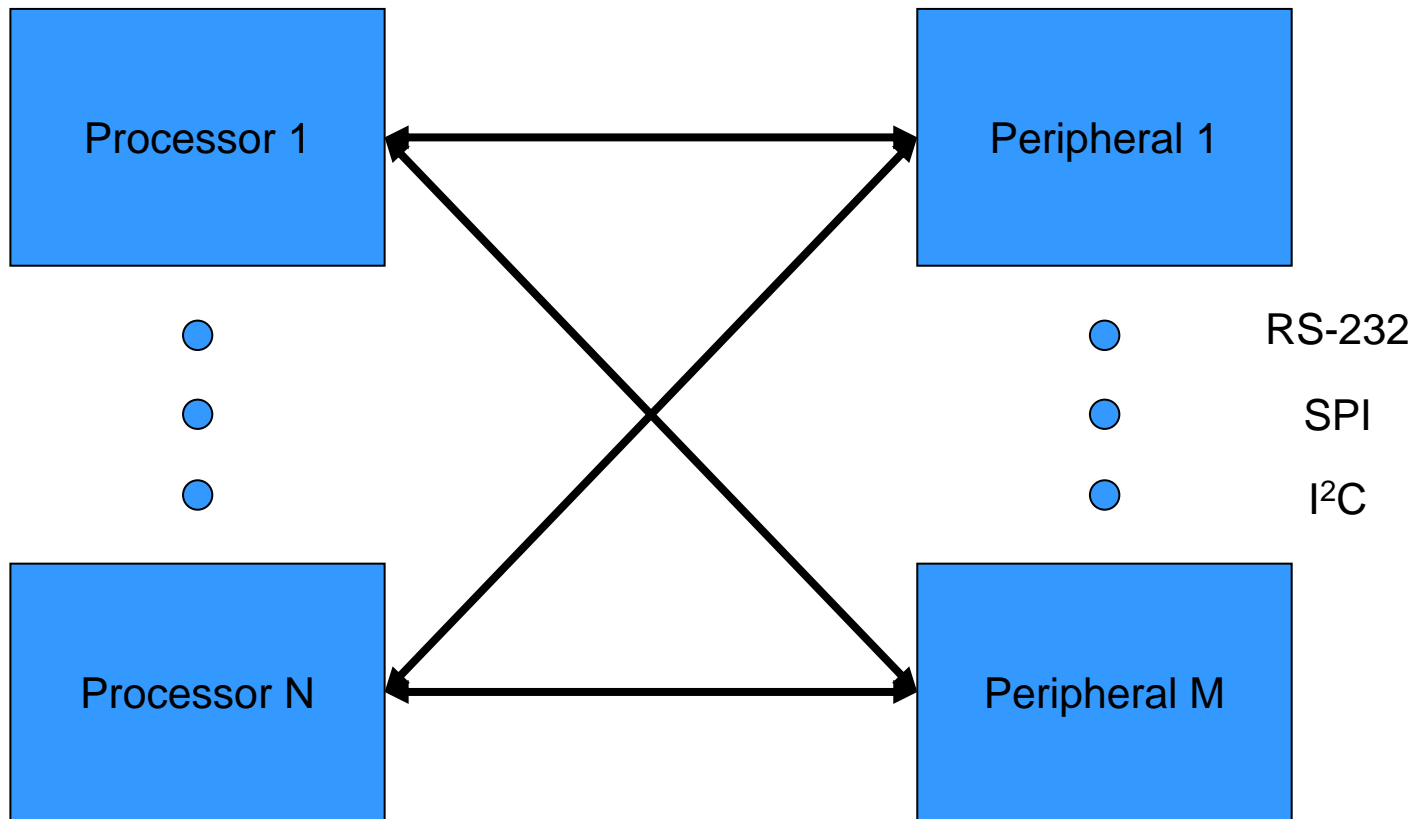
Inter-process Communications



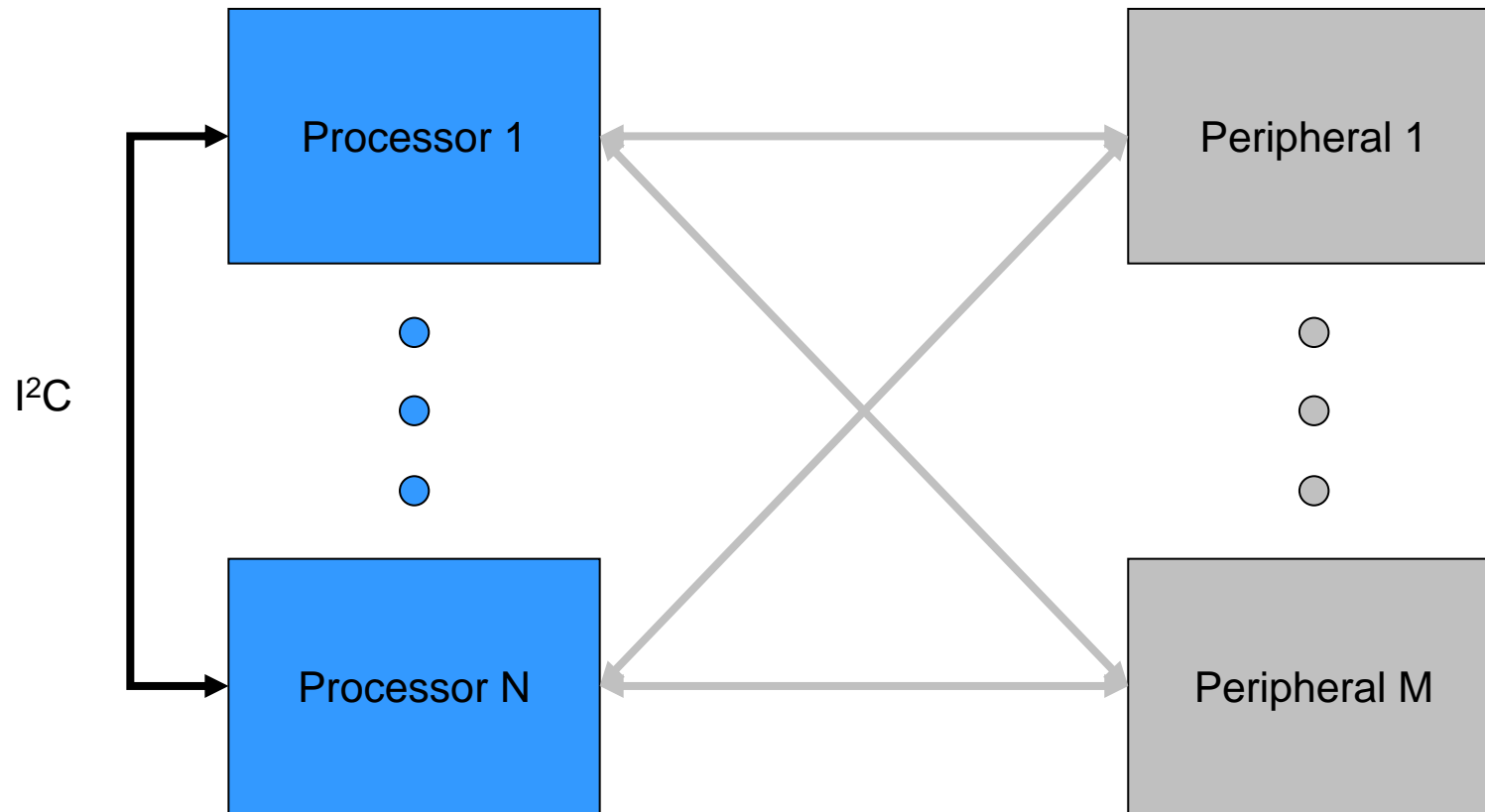
Inter-process Communications



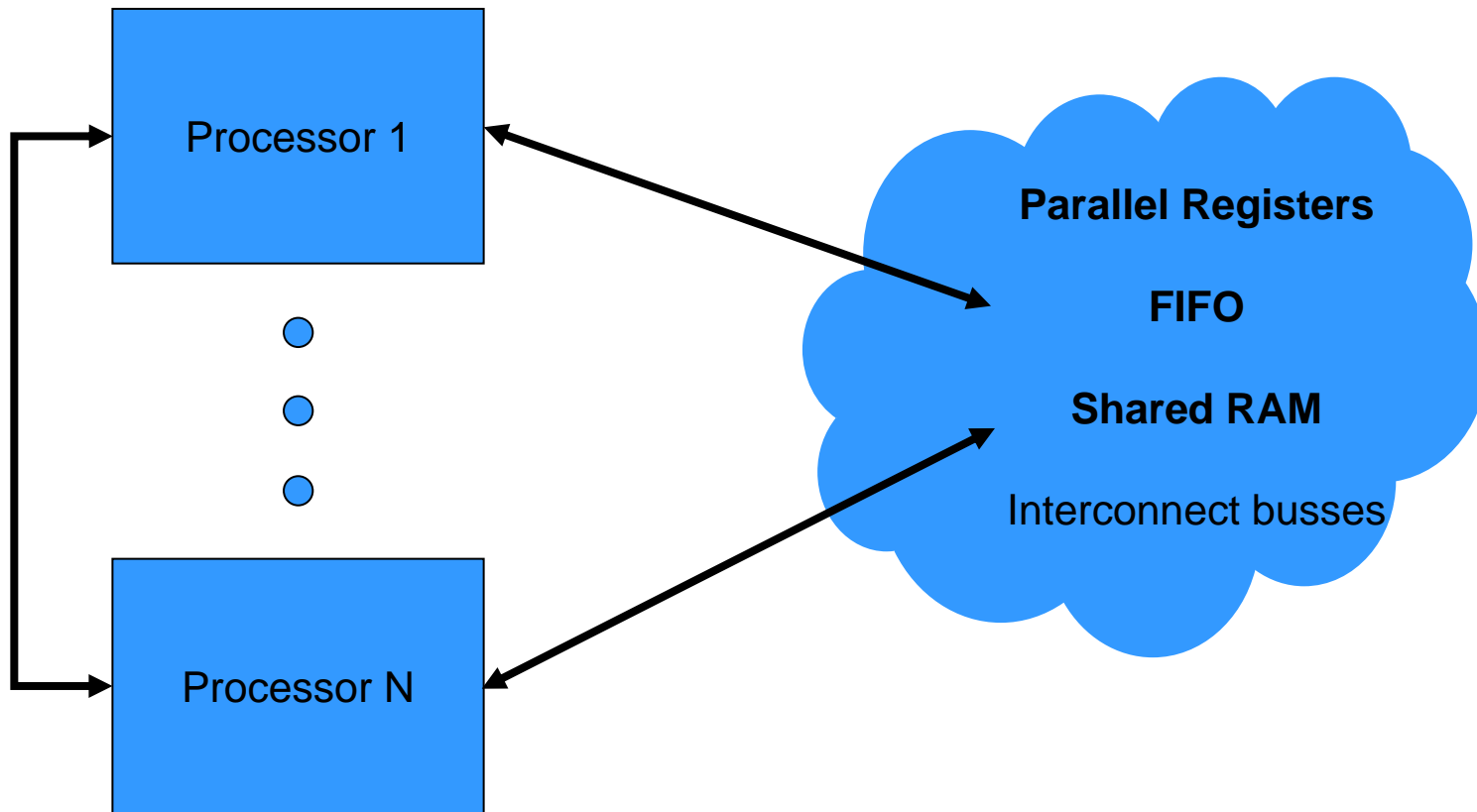
Inter-process Communications



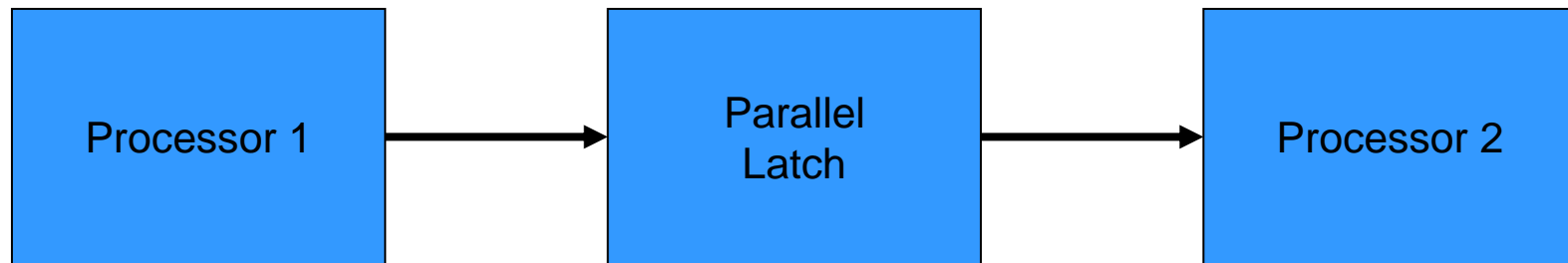
Inter-process Communications



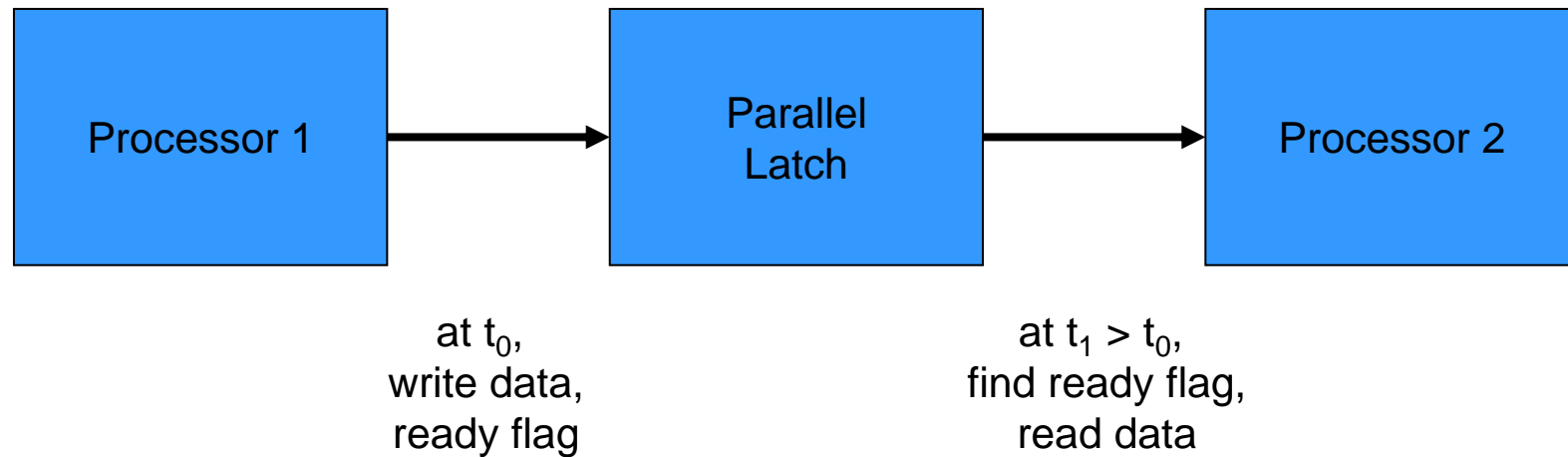
Higher Speed Inter-process Communications



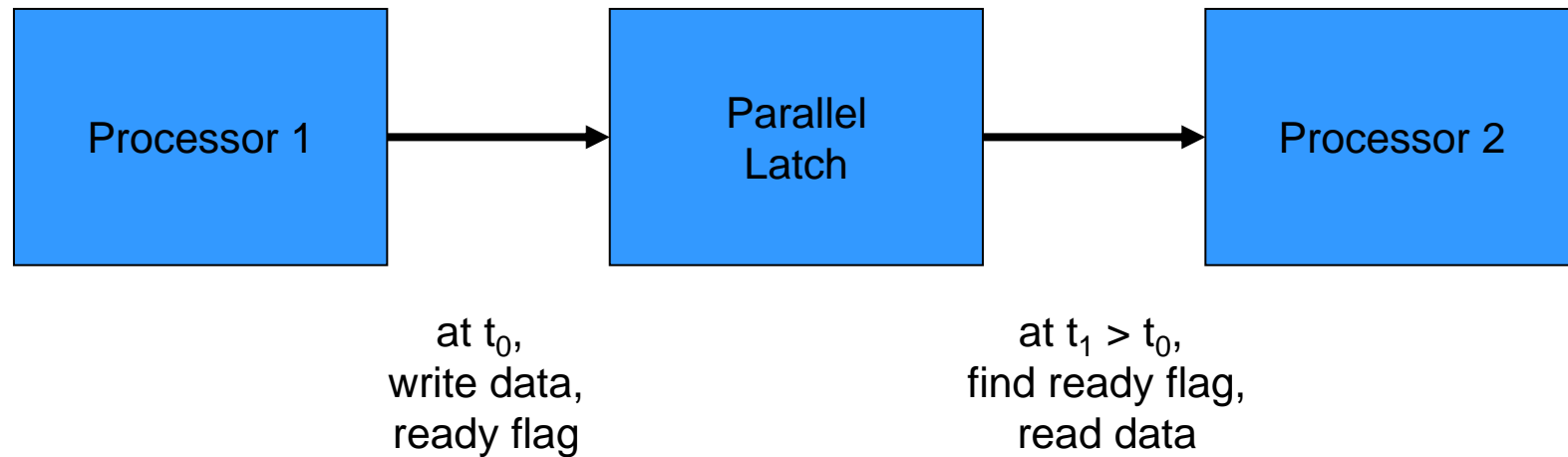
Parallel Register for IPC



Parallel Register for IPC



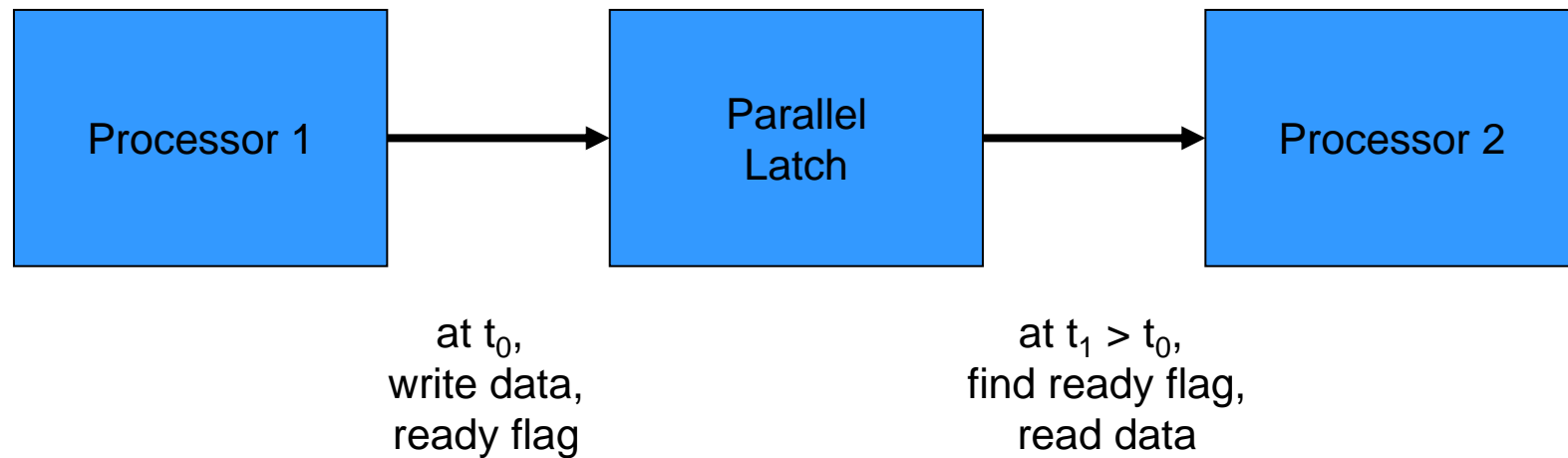
Parallel Register for IPC



Issues:

- One word per transfer
- One latch per processor pair/direction

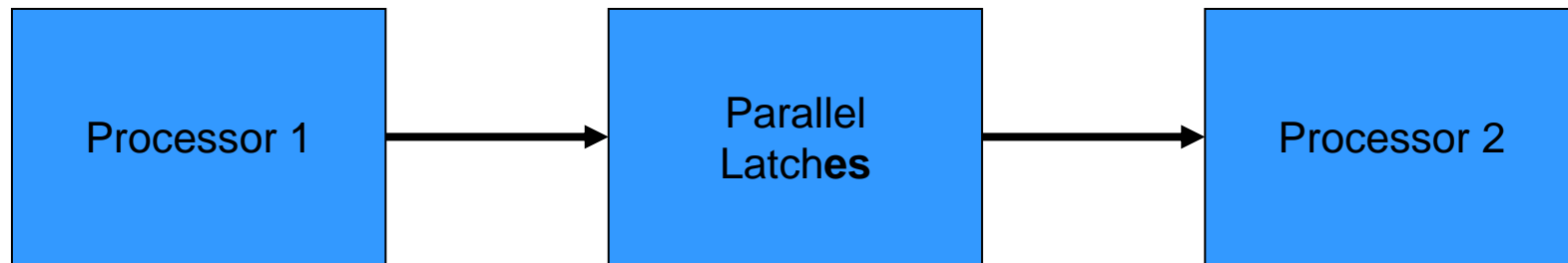
Parallel Register for IPC



Issues:

- One word per transfer – No potential for batch transfers
- One latch per processor pair/direction – N^2 latches are required

Parallel Registers for IPC



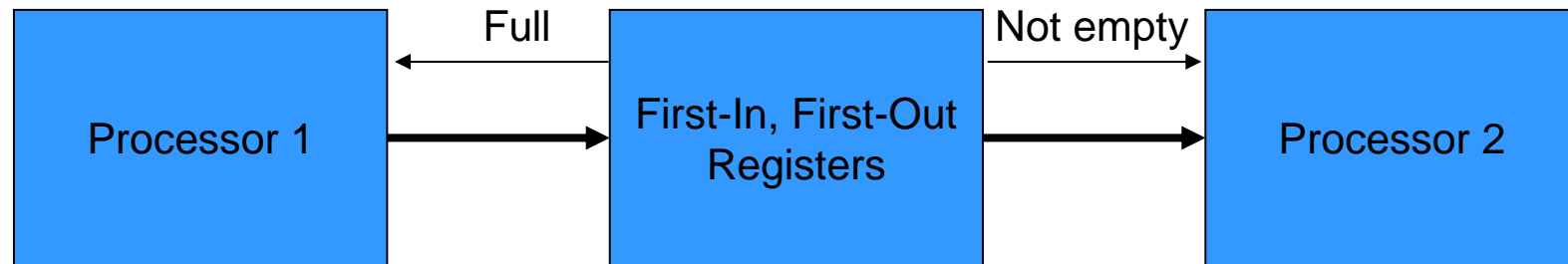
at t_0 ,
write K words of data,
ready flag

at $t_1 > t_0$,
find ready flag,
read K words of data

Issues:

- One word per transfer – ~~No potential for batch transfers~~
 - Restrictive interface (always K words to transfer)
- One latch per processor pair/direction – N^2 latches are required

FIFOs for IPC



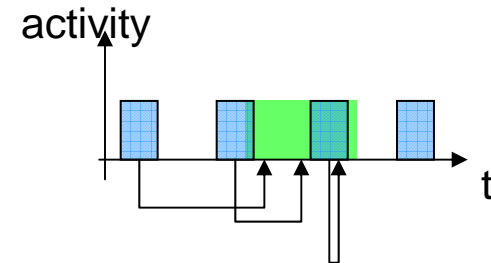
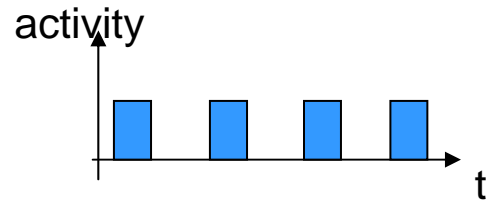
at t_0 ,
write K words of data

at $t_1 > t_0$,
find not-empty flag,
read $J < K$ words of data

Issues:

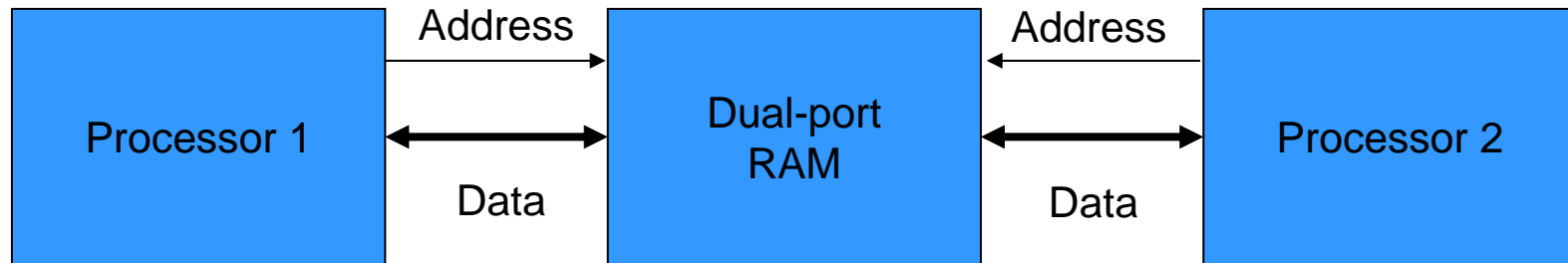
- One FIFO per processor pair/direction – N^2 FIFOs are required

FIFOs as “Elastic Storage” Buffer

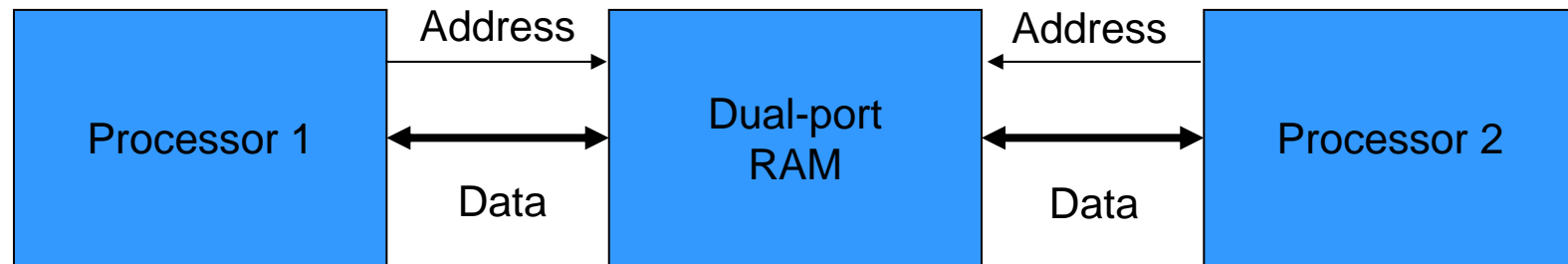


Batch processing can proceed without tight synchronization

“Dual-Port” RAM for IPC



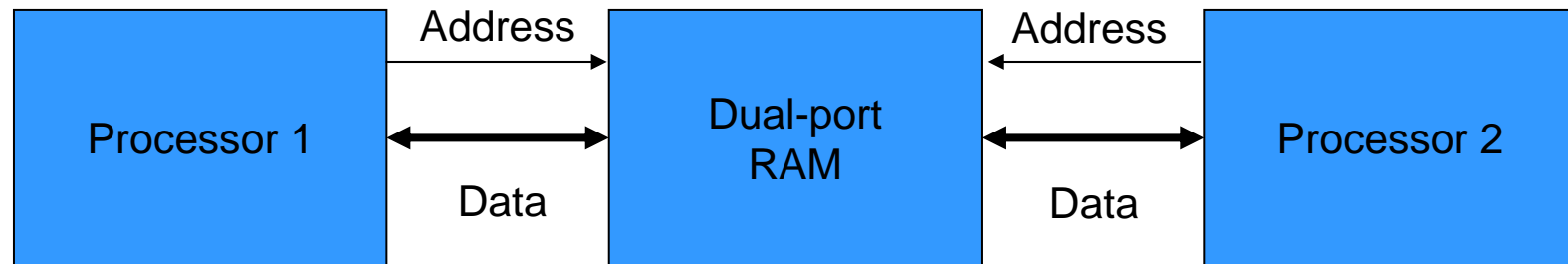
“Dual-Port” RAM for IPC



RAM appears normally in
the address space of P1 and P2

Data and semaphores can be shared

“Dual-Port” RAM for IPC

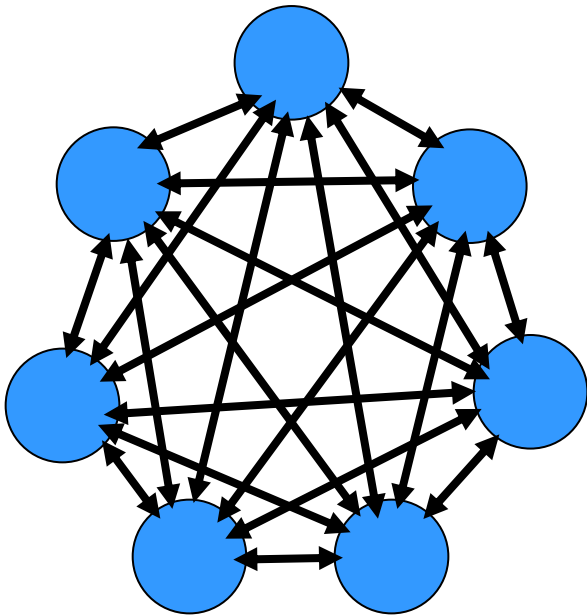


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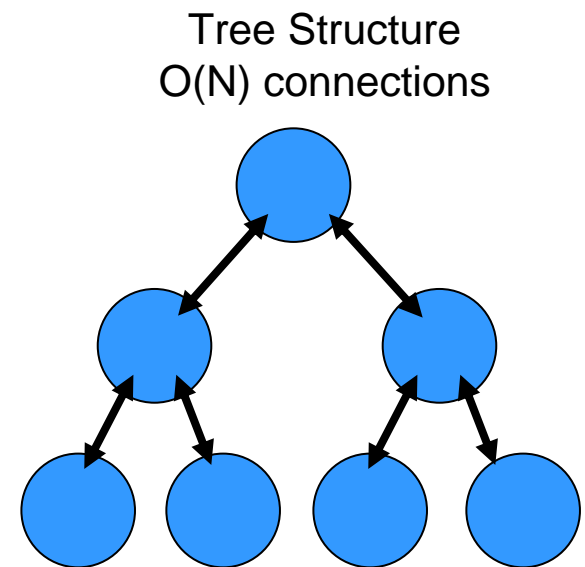
Data and semaphores can be shared

but, $N^2/2$ dual-port RAMs are needed for N processors.

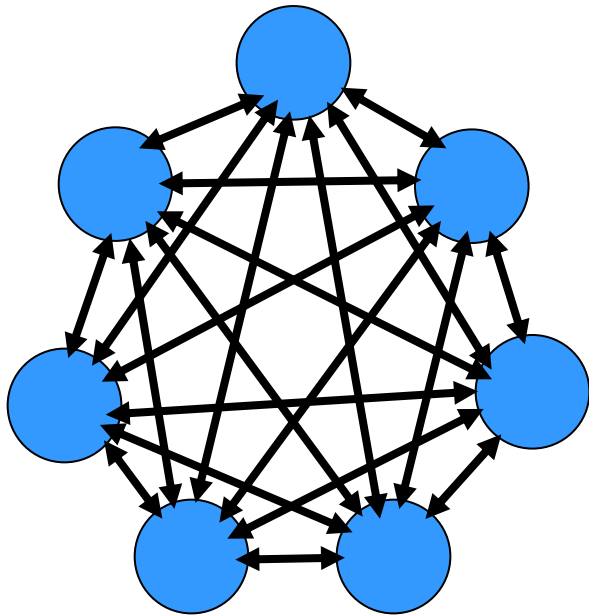
Configurations of Multiprocessing in Embedded Systems



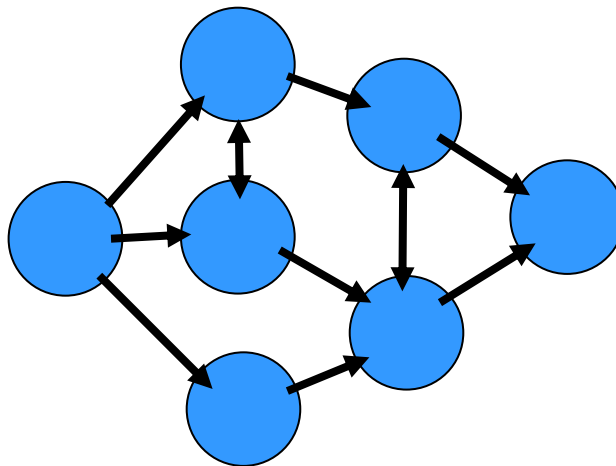
Fully interconnected,
 $O(N^2)$ connections



Configurations of Multiprocessing in Embedded Systems



Fully interconnected,
 $O(N^2)$ connections



More likely configuration
(by careful design?!)

