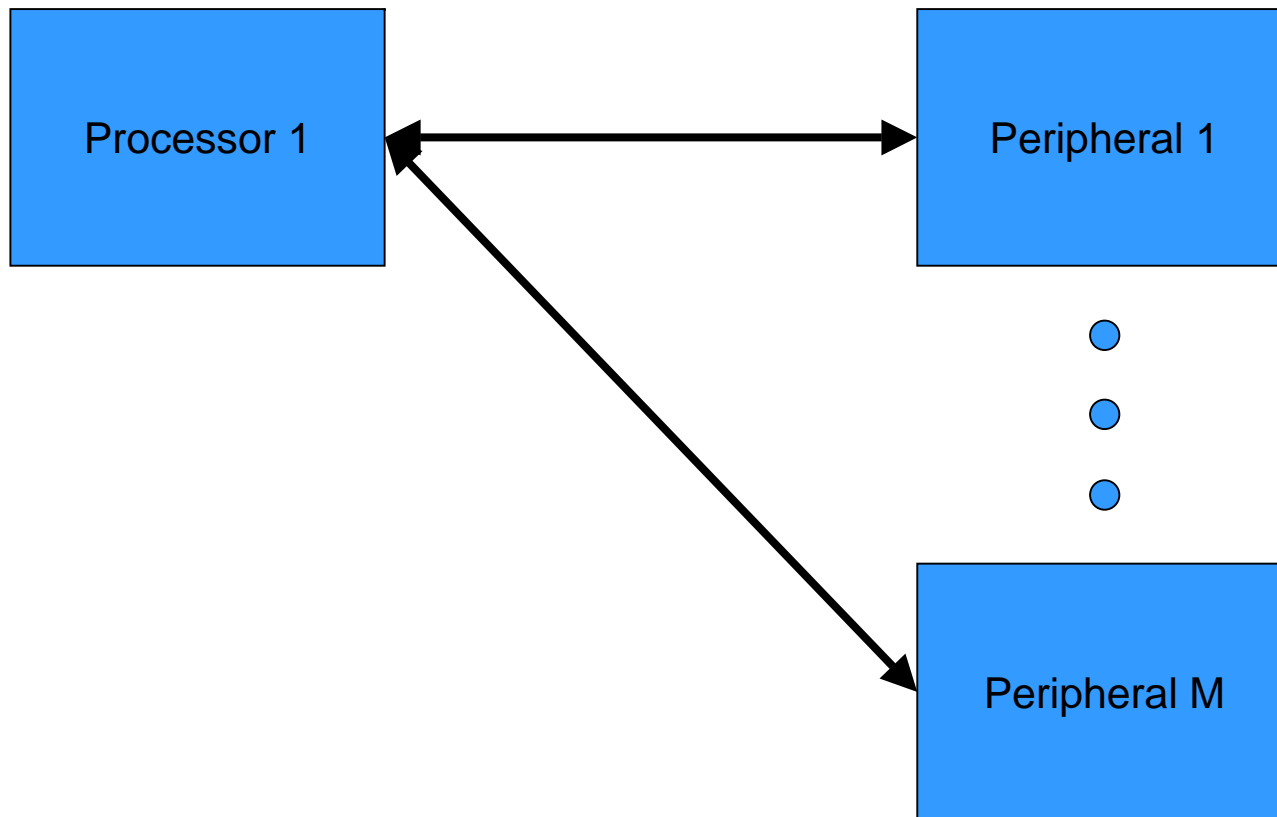


Architecture, Design and Implementation of Embedded Systems for Real-Time Applications

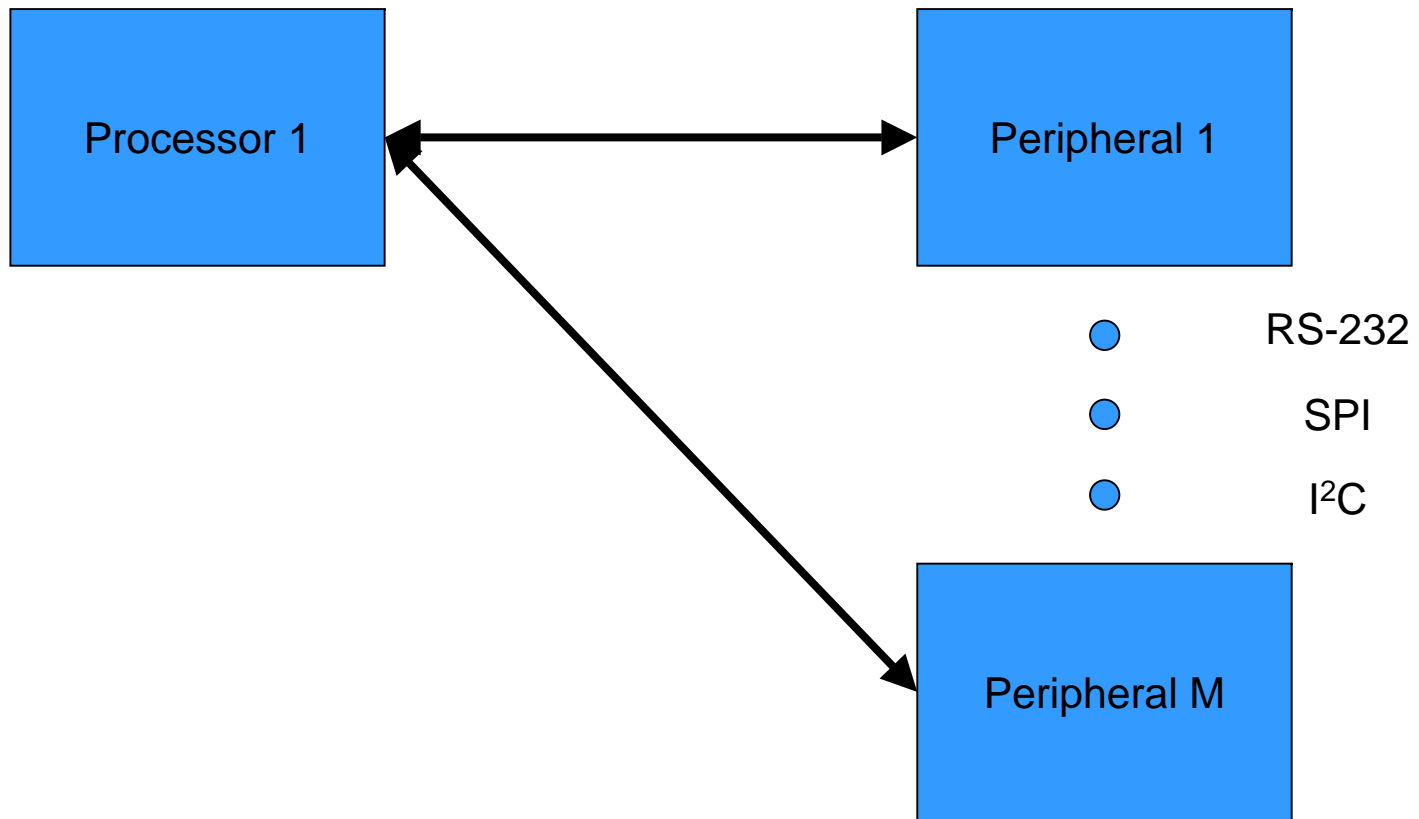
CpE-450 - Spring 05
Class 15

Bruce McNair
bmcnair@stevens.edu

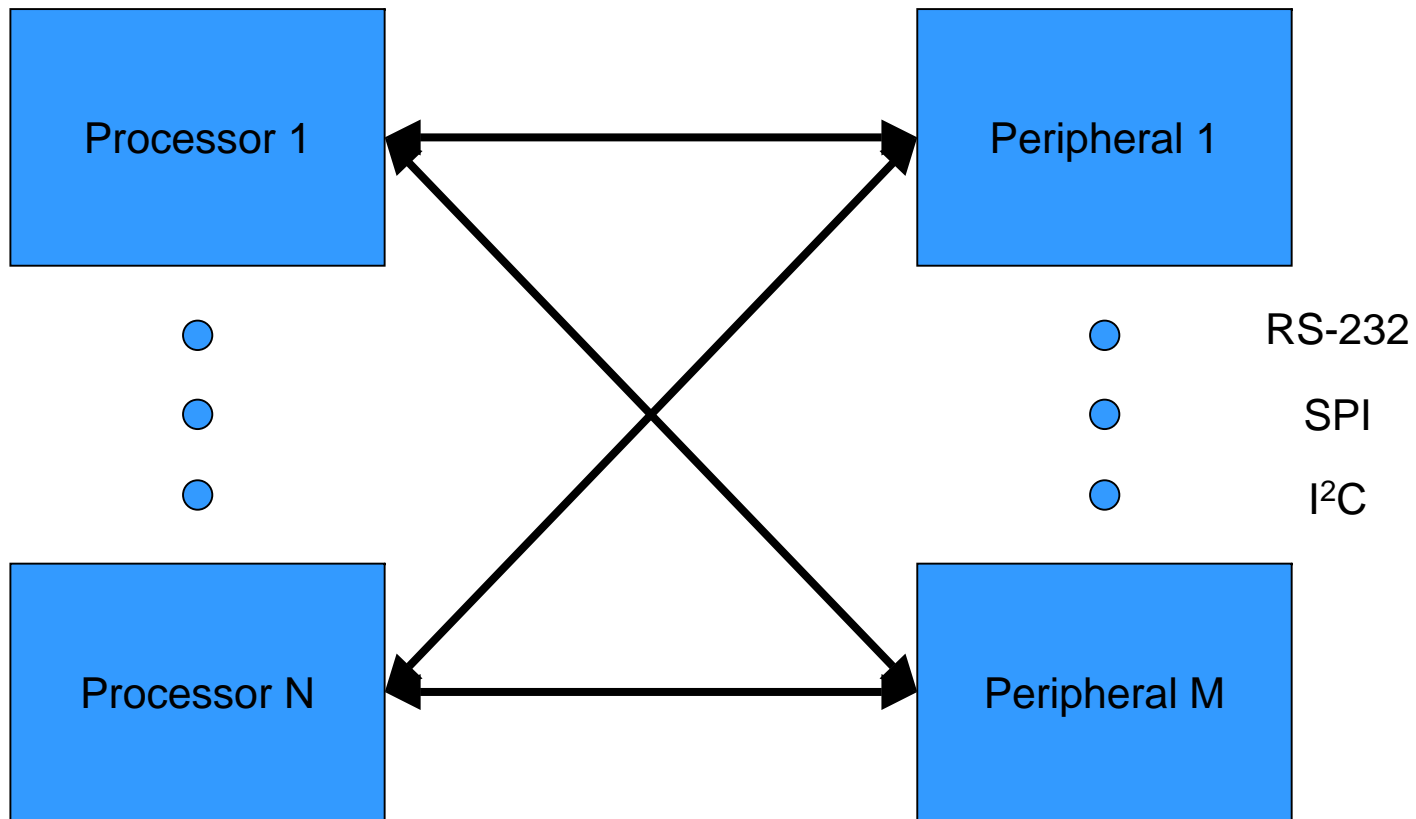
Inter-process Communications



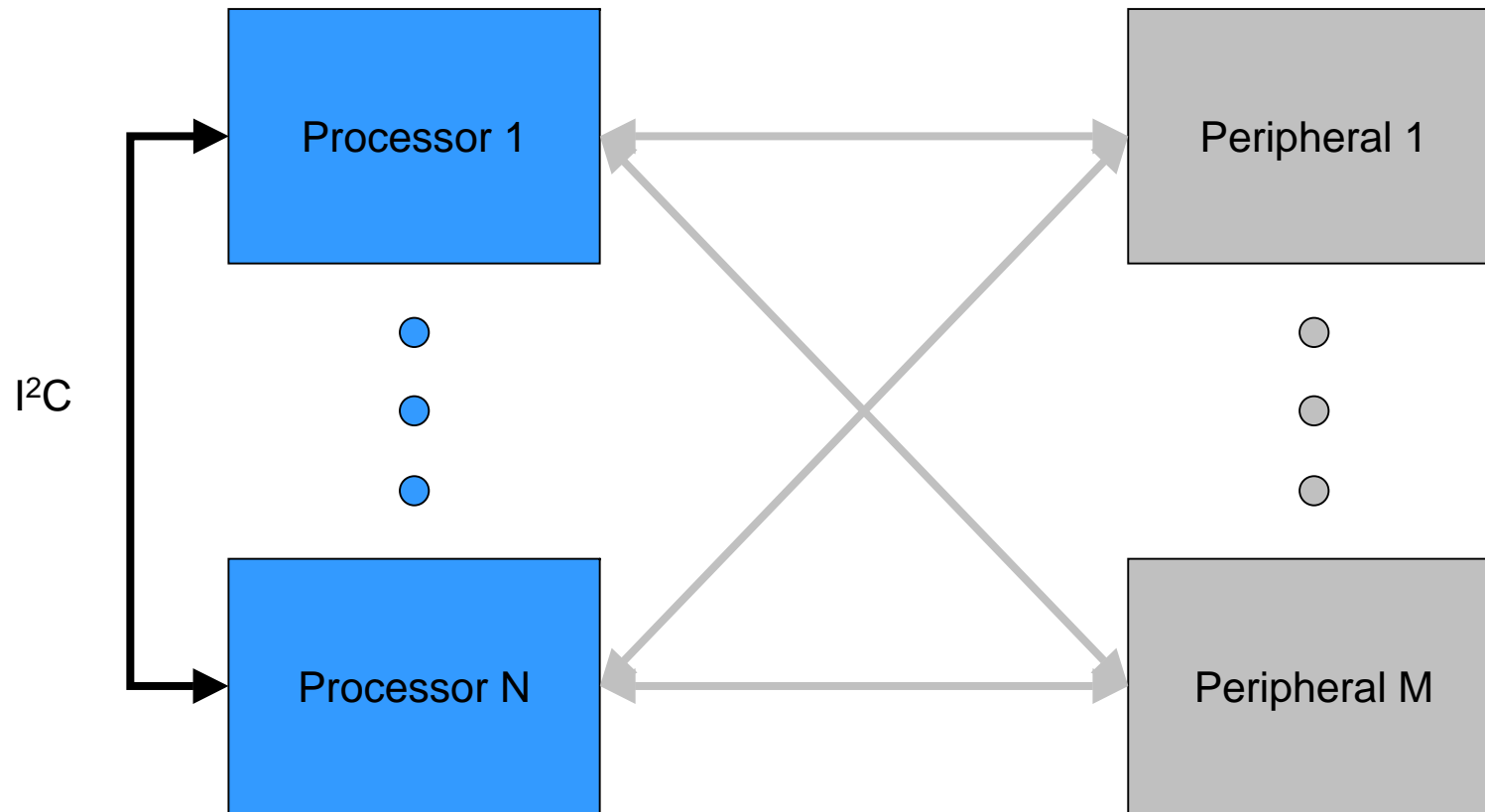
Inter-process Communications



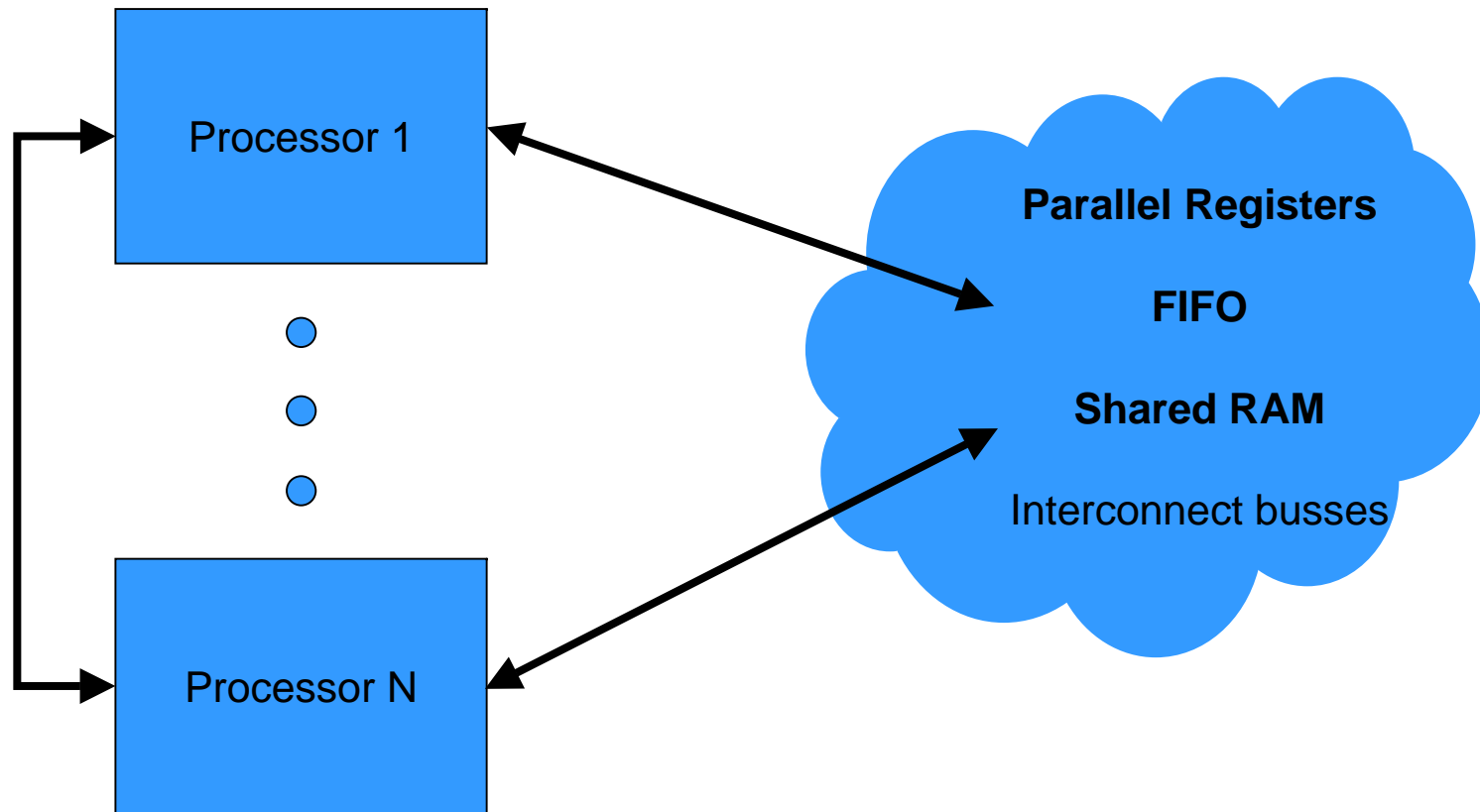
Inter-process Communications



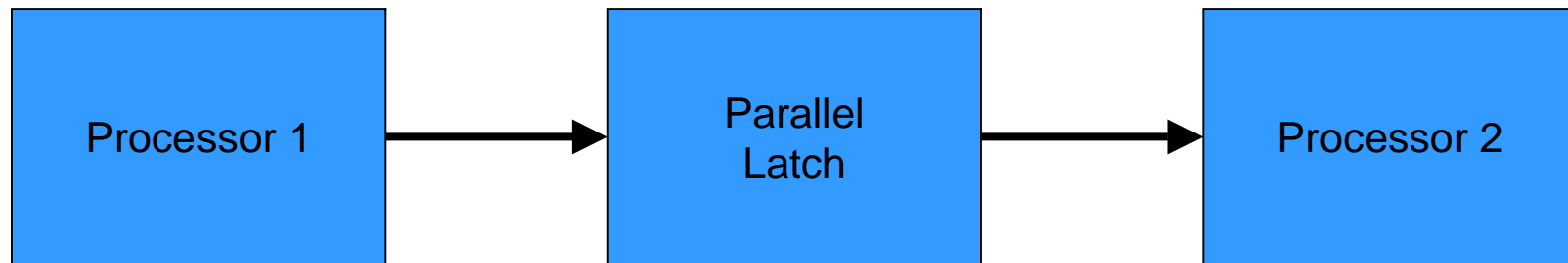
Inter-process Communications



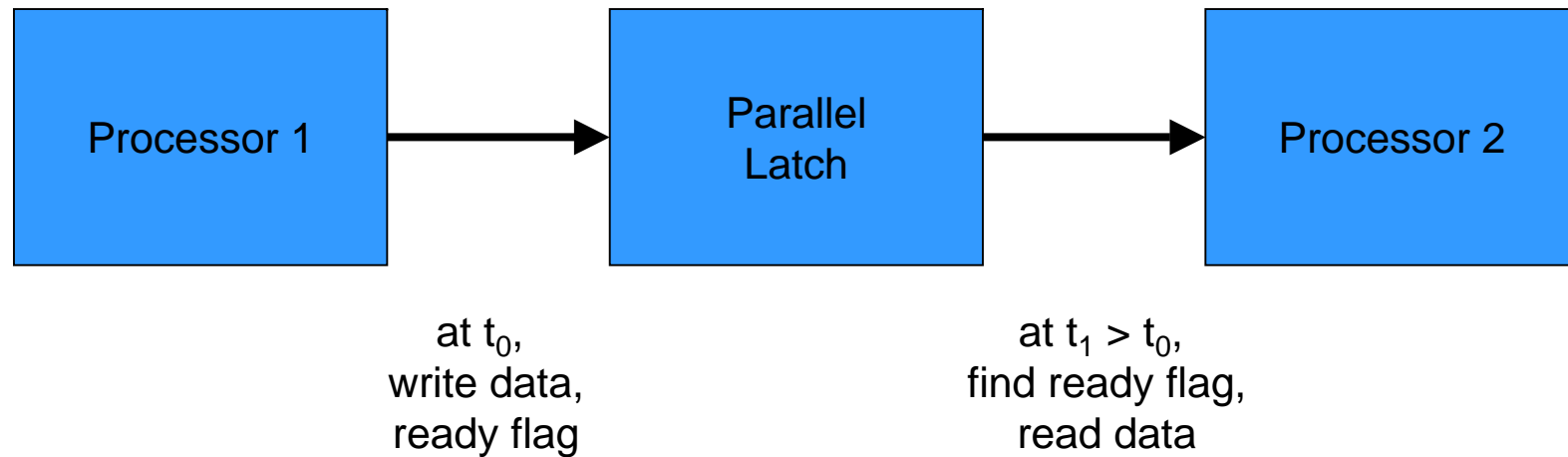
Higher Speed Inter-process Communications



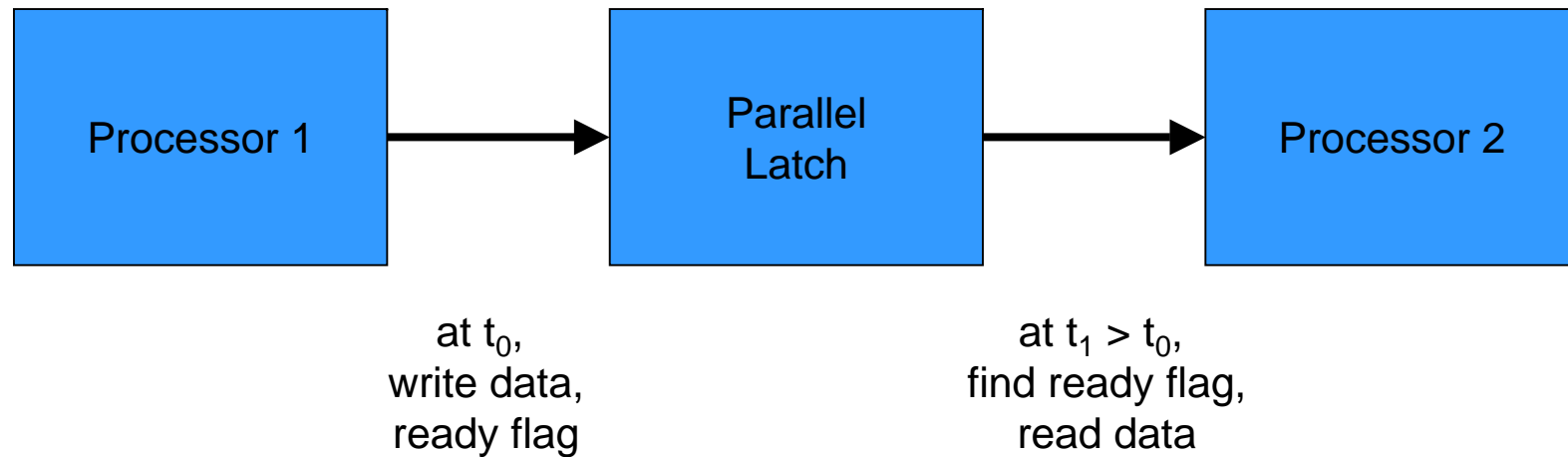
Parallel Register for IPC



Parallel Register for IPC



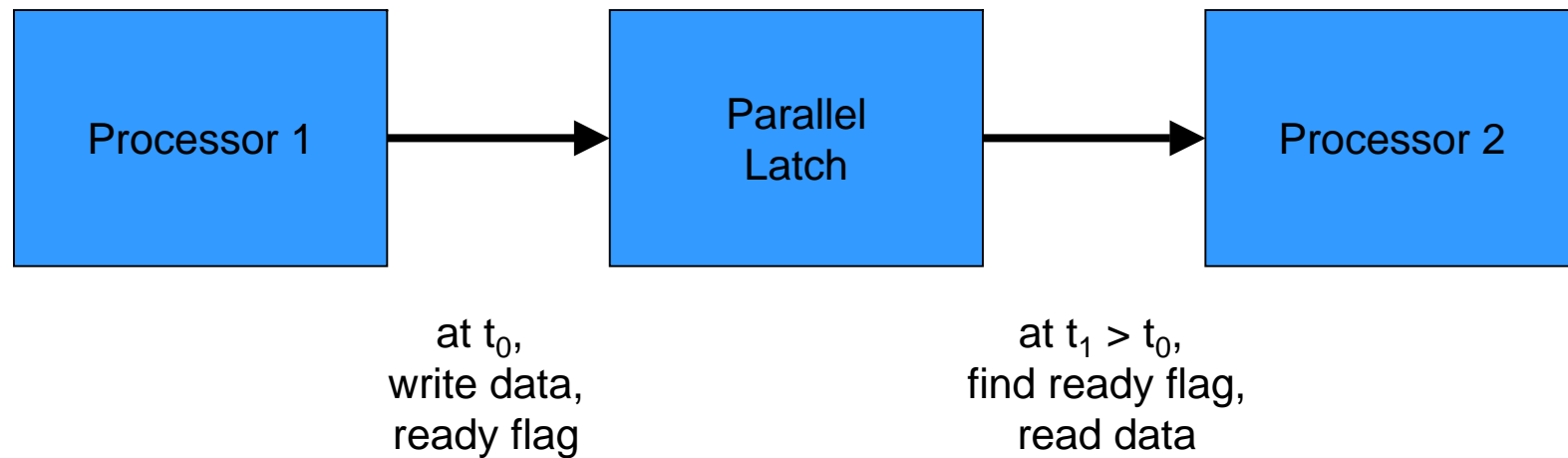
Parallel Register for IPC



Issues:

- One word per transfer
- One latch per processor pair/direction

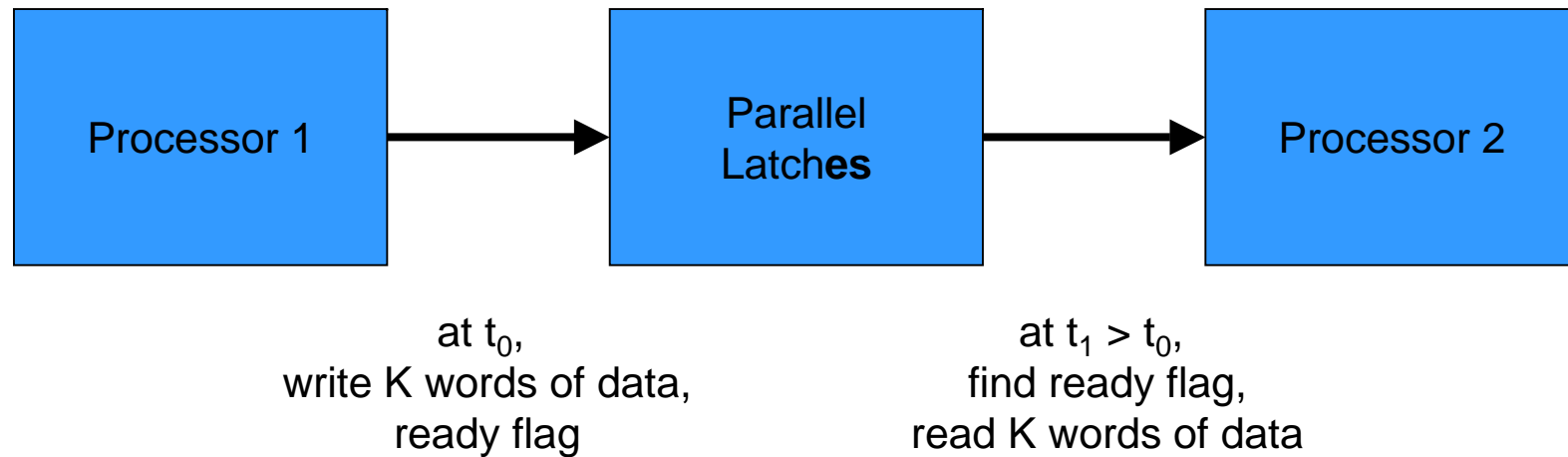
Parallel Register for IPC



Issues:

- One word per transfer – No potential for batch transfers
- One latch per processor pair/direction – N^2 latches are required

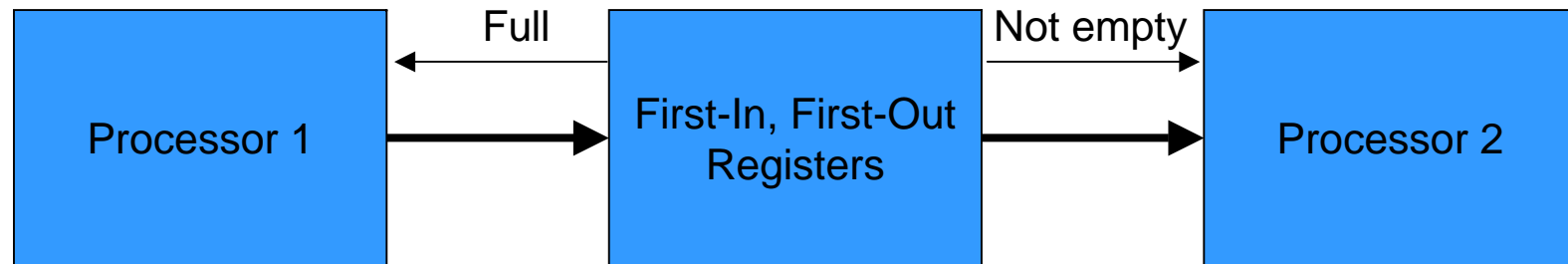
Parallel Registers for IPC



Issues:

- One word per transfer – ~~No potential for batch transfers~~
 - Restrictive interface (always K words to transfer)
- One latch per processor pair/direction – N^2 latches are required

FIFOs for IPC



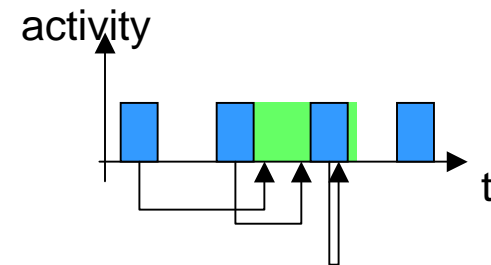
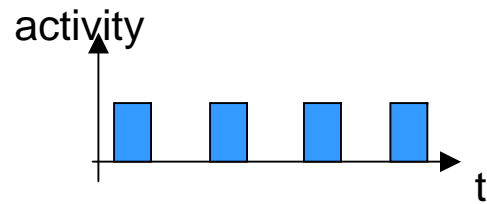
at t_0 ,
write K words of data

at $t_1 > t_0$,
find not-empty flag,
read $J < K$ words of data

Issues:

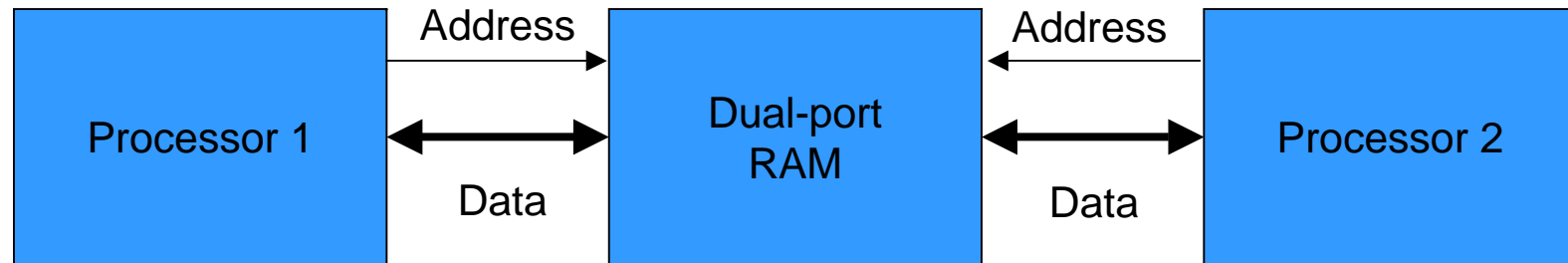
- One FIFO per processor pair/direction – N^2 FIFOs are required

FIFOs as “Elastic Storage” Buffer

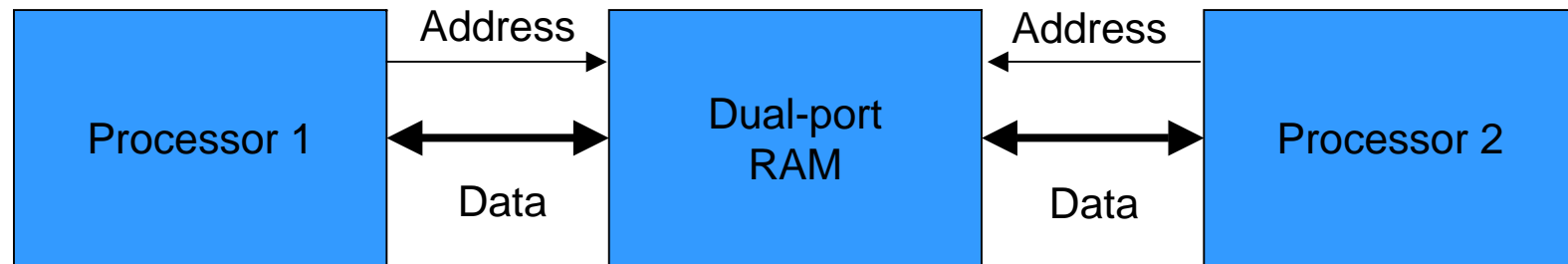


Batch processing can proceed without tight synchronization

“Dual-Port” RAM for IPC



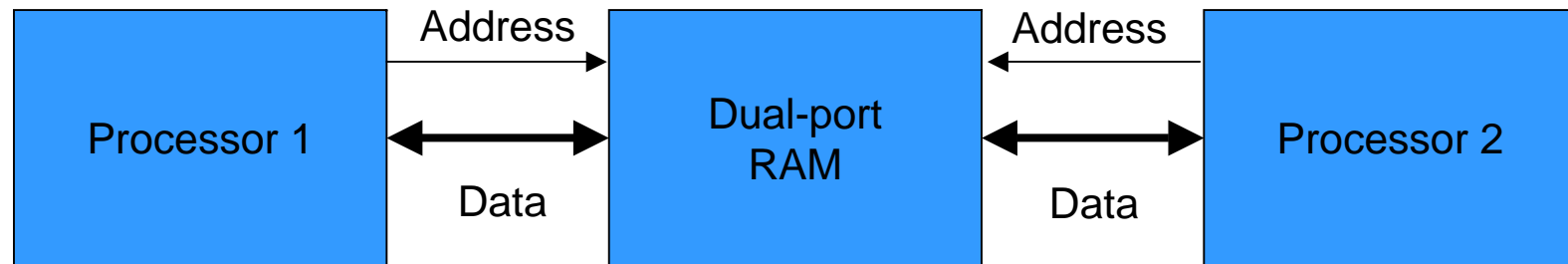
“Dual-Port” RAM for IPC



RAM appears normally in the address space of P1 and P2

Data and semaphores can be shared

“Dual-Port” RAM for IPC

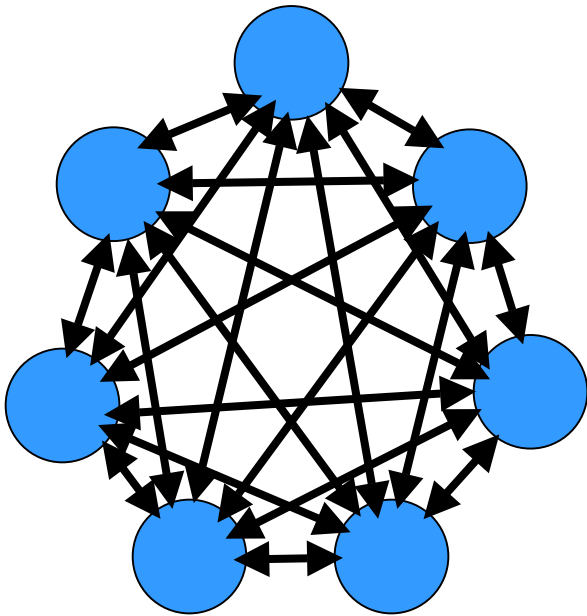


RAM appears normally in
the address space of P1 and P2

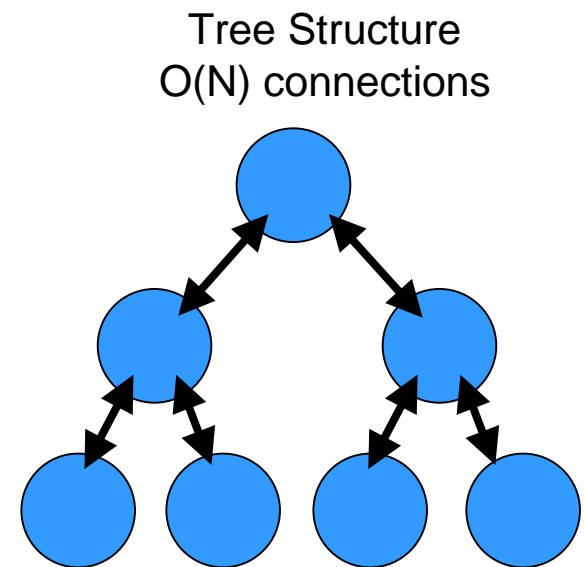
Data and semaphores can be shared

but, $N^2/2$ dual-port RAMs are needed for N processors.

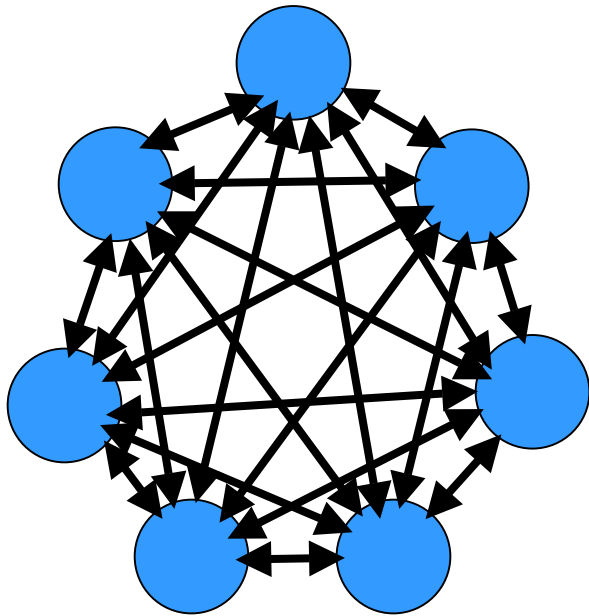
Configurations of Multiprocessing in Embedded Systems



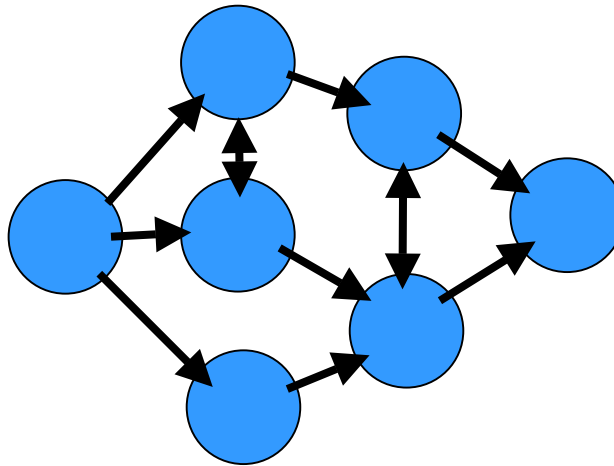
Fully interconnected,
 $O(N^2)$ connections



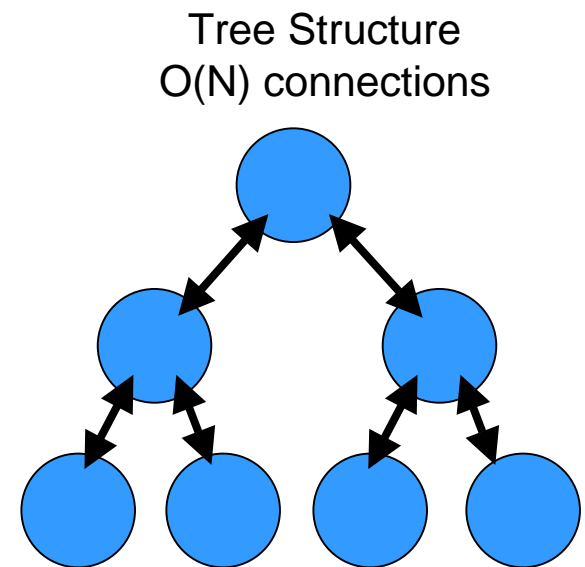
Configurations of Multiprocessing in Embedded Systems



Fully interconnected,
 $O(N^2)$ connections



More likely configuration
(by careful design?!)



Assignment 6

- Dual-port RAM is widely used in multiprocessor systems and semiconductor devices to implement the function have been available for many years. Research the hardware/software structures that can be used to prevent contention when two processors attempt to access the same address simultaneously.
- Whenever two or more processors are accessing the same data independently, there is the possibility that the data one processor sees is not as “fresh” as the data seen by the other processor. Research methods that might be used to deal with this issue.